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Developed Z-Source H-Bridge Multilevel Inverter with Reduced Components for Speed Control of Induction Motor

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ABSTRACT

This paper introduces a new developed H-bridge based cascaded multilevel inverter with reduced components. This topology has a low complexity thereby reducing the overall cost of an inverter. The proposed circuit is connected with a PI controller and switches are controlled by pulse width modulation technique to control the speed of an induction motor. The simulation was carried out using Matlab/Simulink. The simulation of the same was made and performance of various PWM techniques such as Phase disposition (PD), Phase opposite disposition (POD) and phase shifted (PS) and there results were compared on different quantitative measures such as Voltage, current stator Total harmonic Distortion, Voltage stress and rise time. It was observed that that the proposed power circuit with Phase disposition pulse width modulation (PDPWM) that offers reduced total harmonic Detection in terms of voltage, current and phase was found to be very less when compared to other Pulse width modulation techniques. The simulation results will have a fast and quick rise time thereby making this inverter a choice for speed control of induction motor.

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1. INTRODUCTION

Competence of multilevel inverters (MLI) on lower voltage and larger power process that has reduced switching loss, lowered electromagnetic interference, increased quality of the power with reduced harmonics at lower level [1]. DC sources act as an input on set of power semiconductor device connected in an arrangement gives rise to stepped voltage waveform [2]. The MLI has three basic topologies. They are Diode clamped Multilevel Inverter (DCMLI), flying capacitor multilevel inverter (FCMLI), Cascaded Multilevel Inverter (CMLI) [3] [4]. CMLI consists of either symmetric or Unsymmetrical H bridges based on the DC voltage sources. In symmetric type the magnitude of dc voltages of all H bridges are same and for the Unsymmetrical type the voltages differ in H Bridge [5] [6] [7]. Over the years various PWM techniques were used for multi-level inverters.

The renowned PWM methods used for multi-level inverters are the carrier based PWM (SPWM) techniques and the space vector based PWM (SVPWM) techniques. The SPWM schemes are easy to implement and more flexible. These SPWM techniques use a triangular carrier waveform as carrier and sinusoidal signal as reference signal. Multilevel sinusoidal PWM are further classified into carrier and modulating signals. Based on the carrier signals the technique is further classified into Phase disposition (PD), Phase Opposition Disposition (POD), Phase shifted (PS) control technique, super imposed carrier, alternate POD and Hybrid technique.

The various PWM techniques are used on the MLI to achieve desired output with reduced Total harmonic Distortion (THD), voltage stress across switches. An induction motor being rugged, reliable, and relatively inexpensive makes it more preferable in most of the industrial drives. They are mainly used for constant speed applications because of unavailability of the variable-frequency supply voltage [8]-[10]. In this work to increase the output voltage with reduced number of switches is proposed. A novel system for speed control of induction motor is introduced. A closed loop Intelligent Digital controller that acts as a PI controller will furnish the required PWM to control the speed of the induction motor. Different PWM techniques such as PD, POD, and PS were employed on the power circuit and the performance of the system was evaluated using voltage THD, current THD, Stator THD, voltage stress and quick raise time.

Very few researches had attempted to implement the different PWM techniques. This work implements the PD PWM technique for controlling the speed of induction motor. Section 2 gives the working of the New Developed H-Bridge Cascaded multilevel inverter [11]. Section 3 illustrates the Block diagram for the new developed H-Bridge cascaded Multilevel Inverter. Section 4 gives the switched inductor with topology used. Section 5 gives the modes of operation and operating principle. Section 6 illustrates the different PWM techniques used for simulation of the proposed power circuit. Section 7 gives the simulation results and discussions of the power circuit fed on induction motor with different PWM techniques. Section 8 gives the Conclusion of the paper.

2. NEW DEVELOPED H BRIDGE CASCADED MULTILEVEL INVERTER WITH REDUCED COMPONENTS

A Novel new developed H Bridge based cascaded multilevel inverter is proposed. The power circuit will require less number of DC sources and switches. The topology consists of lower blocking voltage on switches, which results in decreased complexity and total cost reduction of the inverter. The Single Phase Seven Level Z –Source Cascaded H-Bridge Multilevel Inverter for seven level inverter is shown in Figure 1.

The Power circuit consists of six unidirectional power switches (Sa_1… Sa_6) and DC Voltages $Vdca_1$ & $Vdca_2$. The switches Sa_1… Sa_2 (or Sa_3… Sa_4) simultaneously turn-on , which causes the voltage sources to short circuit. Therefore, the simultaneous turn-on of the mentioned switches to be avoided. In addition, Sa_5 should be not be turn on at the same time. Figure 2 show the operating sequence of the single phase H bridge multilevel inverter.

Table 1 shows the Switch states and output voltages of the proposed inverters for different states of the switches. In this Table, 1 and 0 indicate the ON and OFF states of the switches, respectively Therefore the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltages sources. The magnitude of $Vdca_1$ and Vdc a_2 should be considered 3 times and 1 time respectively. Similarly, for the topology shown in Figure 1, the magnitude of Vdca1 and Vdca2 should be considered 2 times and 1 times respectively as shown in (1-2).

$$Vdc\ a_1 = Vdc \quad (1)$$

$$Vdc\ a_2 = 3\ Vdc \quad (2)$$

Considering the above equations and parameters in the Table 1, the proposed new developed cascaded seven level inverter can generate 0 +/-Vdc, and 3 Vdc at output.

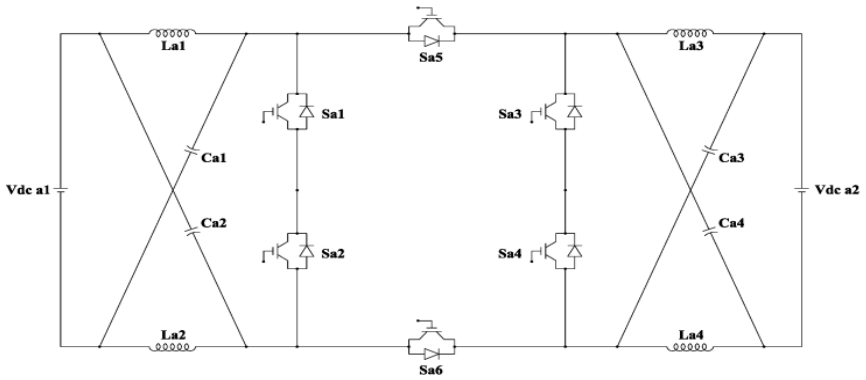

Figure 1. Single phase seven level Z-Source cascaded H-Bridge multilevel inverter

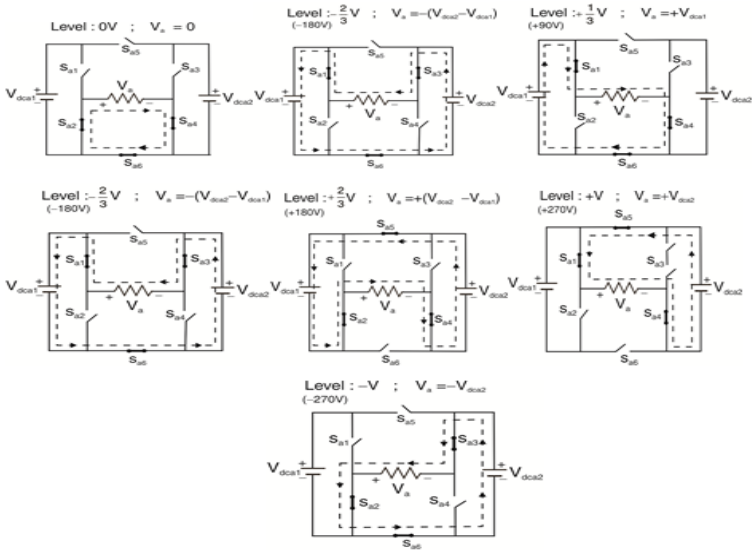

Figure 2. Operation sequence of the single phase seven level Z–Source cascaded H-Bridge multilevel inverter

Table 1. Switch States for the Proposed New Developed H-Bridge Cascaded seven level inverter

Sno	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Vo
1	1	0	0	1	0	1	**Vdca1**
2	1	0	0	1	1	0	**-Vdca2**
3	1	0	1	0	0	1	**Vdca2+Vdca1**
4	1	0	1	0	1	0	**0**
	0	1	0	1	0	1	
5	0	1	0	1	1	0	**-Vdca1**
6	0	1	1	0	0	1	**-Vdca2**
7	0	1	1	0	1	0	**-(Vdca2+Vdca1)**

3. BLOCK DIAGRAM FOR THE PROPOSED H BRIDGE MULTILEVEL INVERTER

The Block diagram of the New Developed Cascaded Seven level Inverter is appeared in Figure 3. It comprises of a Two DC sources with Z-Source, Developed H Bridge inverter, 3rd harmonic injection with SPWM pulse generator along with PI controller with set speed Units. Ccarrier disposition have been introduced through PWM signals are fed to the developed H bridge inverter, which the speed control of the induction motor is achieved [12].

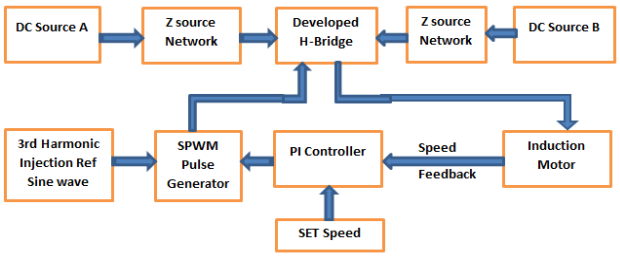

Figure 3. Block diagram of the new developed H-Bridge cascaded multilevel inverter

4. SWITCHED INDUCTOR NEW DEVELOPED Z-SOURCE H BRIDGE CASCADED MULTILEVEL INVERTER TOPOLOG

This topology has wide difference from view of existing structures. It has got the initial solution for the conflicts caused by Modulation Index and D, for the high power quality and high boost invention ability [13] [14]. The new seven level Inverter consists of individual Z-source modules connected to single phase new H Bridge and are cascaded among each other as shown in Figure 4 [15]. For the purpose of explanation the power circuit was explained with one basic Z-source unit connected with one side of the new developed

H Bridge with voltage of Vdc and another Z-source unit connected with other side of H bridge with voltage source of 3 Vdc [16]. Each basic Z-source unit consists of one voltage source and two capacitor (C1& C2) and inductor (L1 & L2) connected as X shape and two switched inductor cells (top cell & Bottom cell), one at the top of the z-source and the other at the bottom of Z-Source module. The DC voltage can be acquired from the rectifier along with Z source network. The seven level yield waveform is acquired by various switching combinations. The switching pattern for three phase seven level topology of the new developed H-Bridge cascaded multilevel inverter is shown in Table 1.

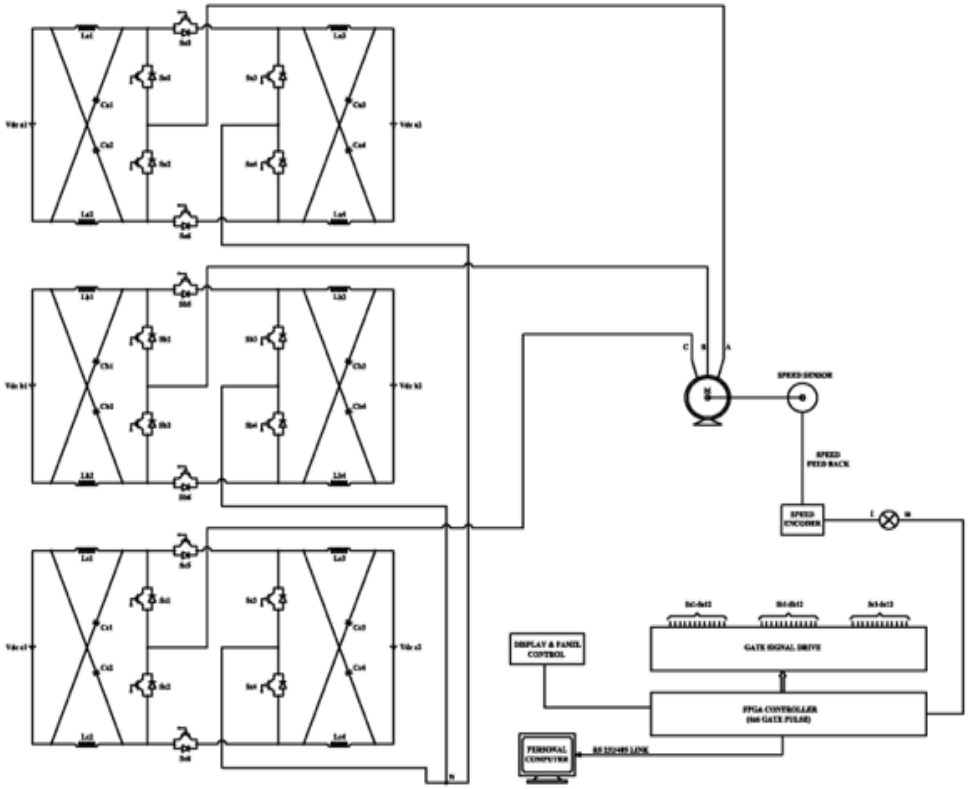

Figure 4. Closed loop circuit diagram for new developed seven level cascaded H Bridge inverter

5. MODES OF OPERATION (OPERATING PRINCIPLE)

The shoot through states in Z-source multilevel inverter are further divided into full shoot through (FST), Upper shoot through (UST) and Lower shoot through (LST). These shoot through switching states are explained by considering one phase leg of multilevel inverter shown in Figure 1. There are three kinds of switching states which generates three kinds of levels as Positive, negative and Zero. In Table 1, Switch ON and OFF positions are indicated with logic 1 and 0 respectively. These shoot through states is allowable in Z-source inverter, because it gives the boosts the DC Link voltage to the inverter.

5.1. Mode 1-Non shoot through mode

The equivalent circuit during non-shoot through mode is shown in Figure 5. An inverter is in a non-shoot through state that is one of the six active states and two traditional open zero states and inductor current meets the following inequality (3):

$$i_L > 0.5\, I_i \quad I_L > 0.5 I_i \tag{3}$$

In this mode, the input DC current as shown in (4):

$$I_{in} = I_{L1}+I_{C1} = I_{L1}+(I_{L1}-i_1) = 2i_L - i_1 > 0 \quad I_{in} = I_{L1} + I_{C1} = I_{L1} + (I_{L1} - i_i) = 2i_L - i_i > 0 \tag{4}$$

Voltage across the inductor as shown in (5):

$$V_L = V_0 - V_C \quad V_L = V_0 - V_C \tag{5}$$

Where V_0 is the source voltage and Inductor current linearly decreases.

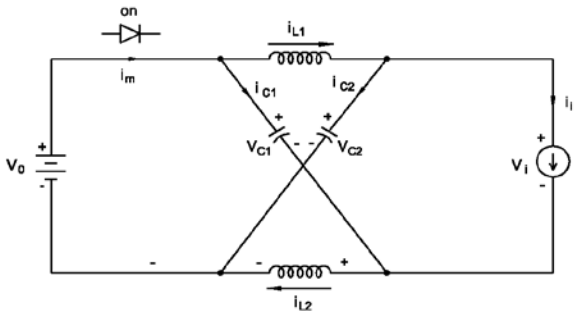

Figure 5. Non Shoot through Mode equivalent circuit

5.2. Mode 2-Shoot through mode

The equivalent circuit in shoot through mode is shown in Figure 6. A switch shoot-through zero state occurs when the switches in any of the three phase legs are gated simultaneously.

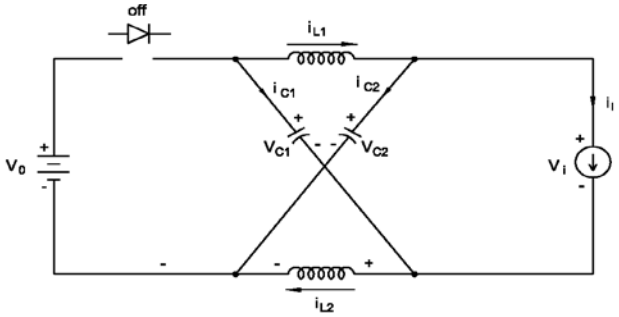

Figure 6. Shoot through mode equivalent circuit

This mode produces a zero voltage vector at the inverter output like open mode and contributes to the total active length of zero voltage state. In this mode (6):

$$V_{C1}+V_{C2}>V_0 \tag{6}$$

The diode is reverse biased, and the capacitors charge the inductors. The Voltages across the inductors as shown in (7):

$$V_{L1}=V_{C1} \text{ and } V_{L2} = V_{C2} \quad V_{L1} = V_{C1}\ V_{L2} = V_{C2} \tag{7}$$

The inductor current linearly increases.

6. PWM TECHNIQUES

Over the years various PWM techniques were used for multi-level inverters. The renowned PWM methods used for multi-level inverters are the carrier based PWM (SPWM) techniques and the space vector based PWM (SVM) techniques. The SPWM schemes are easy to implement and more flexible. These SPWM techniques use a triangular carrier waveform as carrier and sinusoidal signal as reference signal. Multilevel sinusoidal PWM are further classified into carrier and modulating signals. Based on the carrier signals the technique is further classified into Phase disposition (PD), Phase Opposition Disposition (POD), Phase shifted (PS) control technique, super imposed carrier, alternate POD and Hybrid technique [17].

6.1. Phase Disposition PWM technique(PD)

In this method all the carriers have the same frequency and amplitude. Also, the N-1 carriers are in phase with each other. This method uses N-1 carrier signals to generate N level inverter output voltage. All the carrier signals have the same amplitude, same frequency carrier signals have the same amplitude, same frequency and are in phase [4]. Fourteen triangular carrier wave forms are compared with one sine wave. In Figure 7 is illustrates the Phase Disposition Carrier Control Technique.

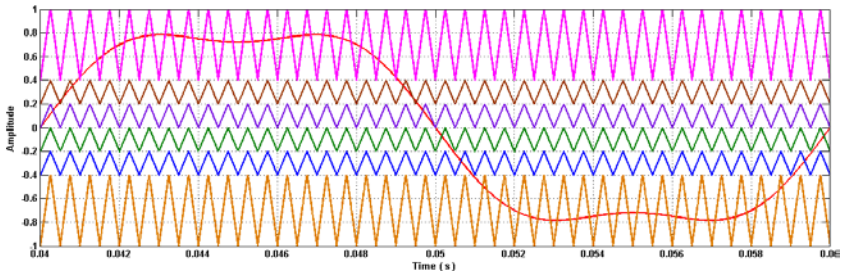

Figure 7. Phase Disposition (PD) Carrier Control Technique

6.2. Phase Opposite Disposition PWM (POD)

In this technique, the carrier signals about the zero reference has same frequency, amplitude and in phase to each other [4]. But below the zero axis the carrier signals are phase shifted by 180 degrees. It requires m-1 triangular carrier signals and the reference is sinusoidal in nature. The important harmonics is centered at Fc and other frequencies appear as side bands around Fc. Figure 8 Illustrates the Phase Opposite Disposition Carrier Control Technique.

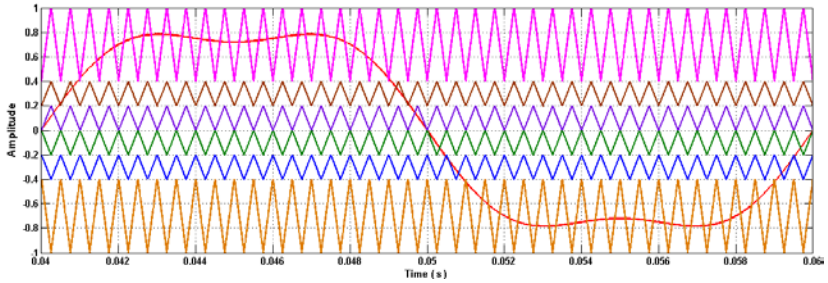

Figure 8. Phase Opposite Disposition (POD) Carrier Control Technique

6.3. Phase Shifted carrier control technique (PS)

In this technique the carrier signals are 90 degrees phase shifted to each other. All the triangular carrier have the same frequency and peak to peak amplitude. For a m voltage level required, m-1 carrier signals are required and they are shifted in phase by an angle θ = (360°/m-1) [17]. Figure 9 Illustrates the Phase Shifted Carrier Control Technique.

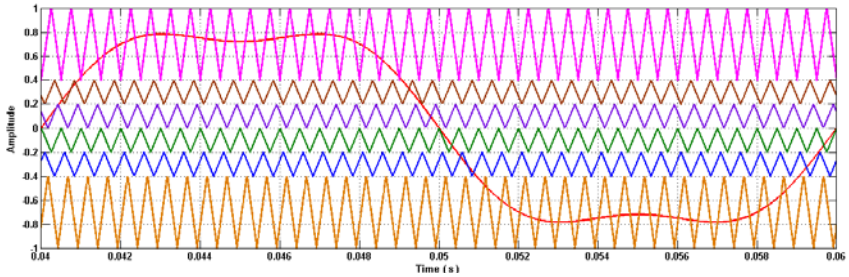

Figure 9. Phase Shifted (PS) carrier control technique

7. SIMULATION RESULTS AND DISCUSSIONS

The proposed power circuit is connected to induction motor with speed of the induction motor is acquired using a speed sensor. The output of the sensor is given to a PI controller that produces desired PWM using the various PWM techniques such as PD, POD, PS. The quantitative parameters such as phase voltage THD, line voltage THD, Stator current THD, settling time and Stress across switches were compared based on the PWM technique applied to the power circuit. The entire simulation was done in MATLAB/SIMULINK and the results are shown below. MATLAB 2013a version was used for all the simulation.

The parameters used for the power simulation on various PWM techniques for seven level cascaded H bridge multilevel inverter. The two different DC link voltage applied to the power circuit are 90 V DC and 270 V DC respectively. The inverter power rating is 200watts with the inverter output voltage is 0-200 V AS RMS (Line to Line) with the switching frequency of 2 KHz. The number of carrier used is three. Figure 10 gives the MATLAB Simulation for Closed loop Circuit Diagram Proposed New Cascaded H Bridge Inverter Figure 11 illustrates the Stator Current in Phase Disposition Carrier PWM Technique.

Figure 12 briefs the Line to Line Voltage for Phase Disposition Carrier PWM Technique. Figure 13 gives the Phase Voltage for Phase Disposition Carrier PWM Technique. Figure 14 illustrates stator current THD, Line Voltage THD, Phase voltage THD in phase Disposition carrier PWM Technique. Figure 15 illustrates Reference Speed and Actual Speed Curve for Phase Disposition Carrier PWM Technique. The proposed hardware with different PWM technique were employed and connected to an induction motor. Speed control of the induction motor is performed. From the exhaustive results tabulated the following were inferred. Various PWM techniques were applied on the power circuit and THD, and Voltage Stress were tabulated. From Table 2, it is clear that the proposed power circuit with Phase disposition PWM exhibits lower phase voltage THD, Line voltage THD, Stator current THD and voltage stress. The PD based power circuit has a phase voltage THD of 29.2%, line voltage of 15.32%, stator current THD of 2.45%, voltage stress of 90V and 270V with a very quick rise time of 0.0965sec. Table 3 shows the Comparison of Two Speed 500/1200 rpm for the Induction Motor with Rise time on the proposed seven level cascaded H-bridge based multilevel inverter is given.

Table 2. Comparison of different measures on various PWM techniques on seven level cascaded multilevel inverter

PWM	PH (V) THD	LINE (V) THD	STA (I) THD	VOL. STRESS
PD	24.52%	13.12%	1.31%	90V & 270V
POD	29.82%	20.58%	2.68%	90V & 270V
PS	29.87%	18.82%	2.60%	90V & 270V

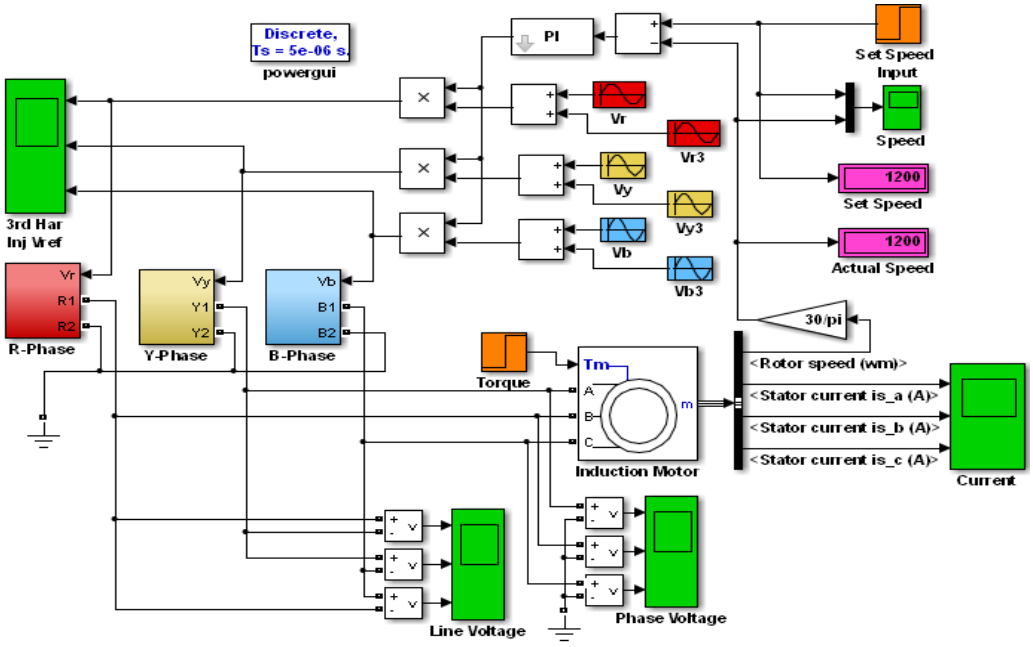

Figure 10. Matlab simulation for new developed h bridge multilevel inverter

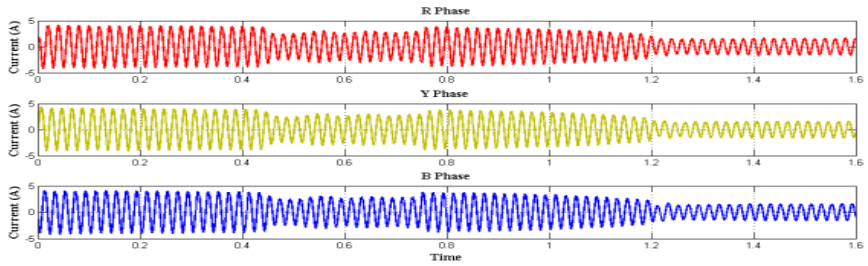

Figure 11. Stator current in phase disposition carrier pwm technique

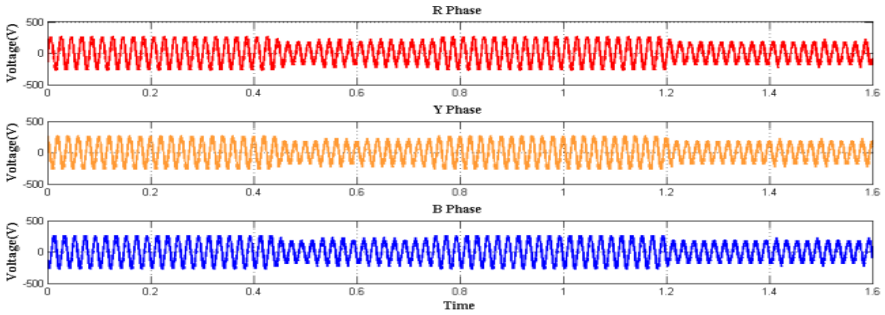

Figure 12. Line to line voltage for phase disposition carrier pwm technique

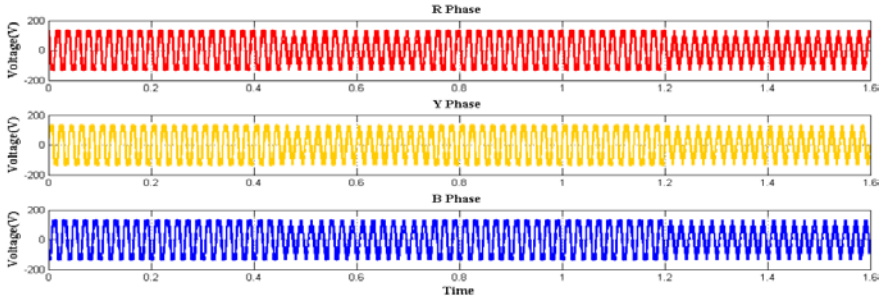

Figure 13. Phase voltage for phase disposition carrier pwm technique

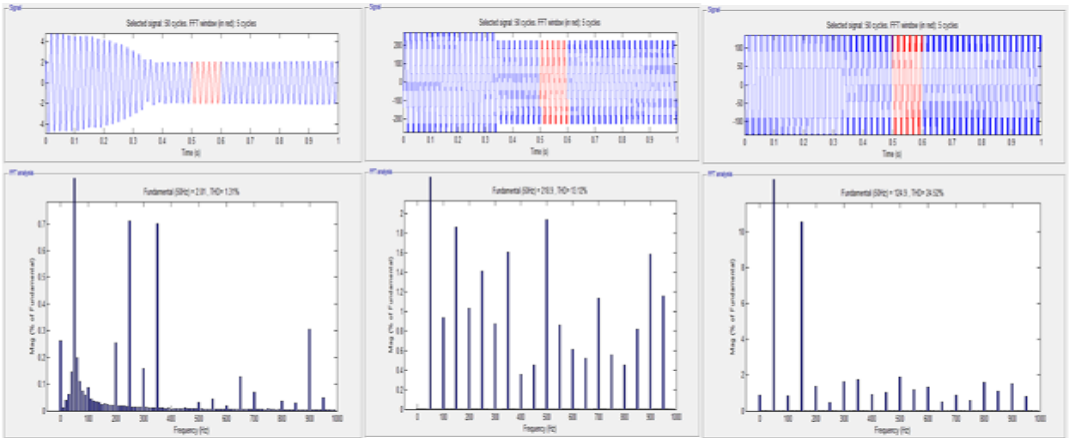

Figure 14. (a) stator current THD (b) Line Voltage THD (c) Phase voltage THD in Phase Disposition carrier PWM Technique

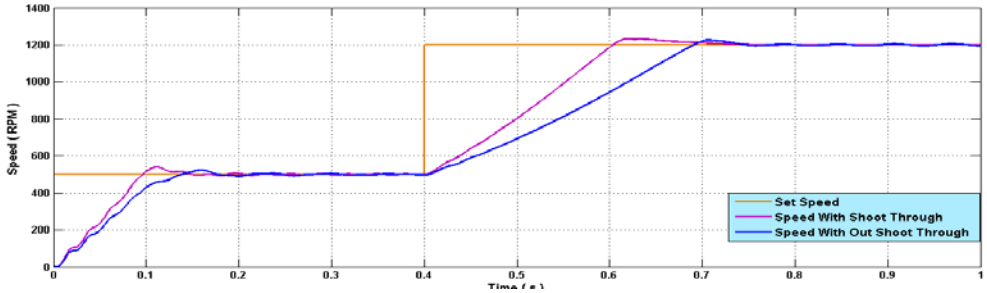

Figure 15. Reference Speed and Actual Speed Curve for Phase Disposition Carrier PWM Technique with shoot through and without shoot through

Table 3. Comparison of Two Speed of Induction Motor with Rise time in Phase Disposition (PD) PWM Technique

Speed Range (RPM)	With Shoot Through Rise Time (S)	Without Shoot Through Rise Time (S)
0-500	0.0965	0.1365
500-1200	02036	0277

8. CONCLUSION

In this work, the phase disposition (PDPWM) control was developed by connecting with reduced number of components and the performance the simulation for the speed control of the induction motor. The combination of the power circuit provides a lower total harmonic distortion in terms of phase voltage, line voltage and stator current. The performance of the proposed circuit was evaluated using THD, voltage stress and settling time. The Simulation settles very quickly with the rise time along with shoot through of 0.0965sec and without shoot through of 0.136sec in Phase disposition (PD) PWM technique. From this analysis it is concluded that THD for PD PWM technique was found to exhibit low THD, creates less voltage stress and settles quickly when compared to other PWM schemes.

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