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Micro controller based asymmetrical multilevel inverter

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ABSTRACT

This paper presents the Asymmetrical multilevel inverter with 1:3 voltage propagation. Switching pulse for Asymmetrical multilevel inverter are generated using embedded controller in m-file using MATLAB. The Asymmetrical multilevel inverter with 1:3 voltage propagation can produce high quality output voltage with less number of switches and voltage sources compare to conventional multilevel inverters. Contrasting other switching schemes, the proposed Switching scheme significantly reduces the Total Harmonic Distortion (THD) and minimize switching losses and reduces the complexity. To evaluate the developed scheme, simulations are carried out through MATLAB and real time implementations are done through microcontroller ARM Cortex™-M0 Core. The simulation and hardware results are presented.

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1. INTRODUCTION

A circuit which converts DC input voltage to AC output voltage of desired magnitude and frequency is called an inverter. Inverters are mainly classified according to the nature of input source as voltage source and current source inverters. The inverters can also be classified according to the nature of output voltage waveform as square wave, quasi square wave and PWM inverters. The inverters can be further classified based on method of connections as series inverters, parallel inverters and bridge inverters. Based on number of phases, the inverters can be grouped as single phase and three phase inverters. Depending on the number of levels in output voltage, inverters can be divided into two categories: two level and multilevel inverters.

The function of a MLI is to synthesize a desired AC output voltage from several DC voltage sources with extremely low distortion. The MLIs provide high output voltages with low harmonics without the use of transformers or series connected synchronized switching devices. MLIs offer several advantages. These include higher DC bus utilization, improved harmonic performance and reduced stress on power devices. The multilevel inverters can be classified into three types. They are Diode Clamped MLI (DCMLI), Flying capacitor MLI (FCMLI) and Cascaded MLI (CMLI). The main drawback of above mentioned conventional multilevel inverters is the need for large number of isolated DC supplies, circuit elements and power electronic switches.

In conventional multilevel inverters the DC voltages of each cell are equal. However it is possible to have unequal DC voltages, which increase the number of voltage levels without increasing the number of switches and such configuration, is called as asymmetrical multilevel inverter. Asymmetrical approach simplifies both the design and the control of the converter structure [1]. The difference between values of sources improves performance of multilevel inverter and enhances the number of levels [2]. Binary DC source seven level multilevel inverter synthesize seven level output with reduced power electronic component compare to conventional multilevel inverter [3]. The trinary one can offer a waveform with 3n

levels, where n is the sum of modules associated in cascade [4]. Operating the main inverter under the fundamental line frequency ensures high efficiency. The main H-bridge to enable transformer less operation without leakage current issue as well as to improve the efficiency in [5]. A single phase trinary DC source nine level inverter topology for investigation with various SPWM switching techniques are presented in [6]. Single phase Trinary DC source nine level inverter topology for investigation with embedded controller switching technique significantly reduces the Total Harmonic Distortion [7]. Hybrid multilevel inverter supplied with different voltage sources and digital control algorithm are implemented using DSP controller and flip-flaps [8-10]. Microcontroller based asymmetrical multilevel inverter in micro-grid applications are discussed in [11]. Multilevel inverter with reduced number of switches and sources are discussed in [12].

This paper focus on embedded controller based Asymmetrical multilevel inverter with 1:3 voltage propagation and real time implementation using microcontroller ARM Cortex™-M0 Core. The proposed inverter can synthesize high quality output voltage near to sinusoidal wave form. The circuit configuration is simple and easy to control.

2. ASYMMETRICAL CASCADED MULILEVEL INVETER

Figure 1 shows a circuit configuration of a asymmetrical cascaded H-bridge multilevel inverter employing trinary dc input source. It looks like a traditional cascaded H-bridge multilevel inverter except input trinary dc sources. The two input source are Vdc and 3Vdc, it can synthesis nine output levels; Vdc, 2Vdc, 3Vdc, 4Vdc, 0, -Vdc, -2Vdc, -3Vdc, -4Vdc.The lower inverter can generate a fundamental output voltage with 3-levels, and then the upper inverter adds or subtracts 1-level from the fundamental wave to synthesize stepped waves. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as (1)

$$V_{out} = V_{HB1} + V_{HB2} \tag{1}$$

In the proposed circuit topology, if n number of DC sources in sequence of the power of 3, an expected output voltage level is given as (2). Figures 2-9 shows the gating pattern generated using embedded control technique.

$$V_n = 3^n, n = 1, 2, 3.. \tag{2}$$

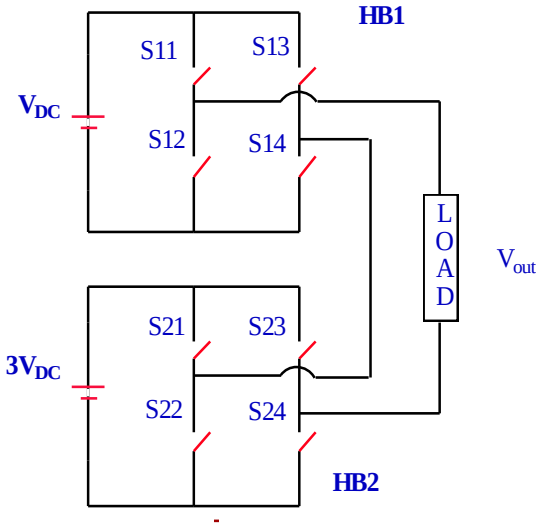

Figure 1. Asymmetrical cascaded multilevel inverter

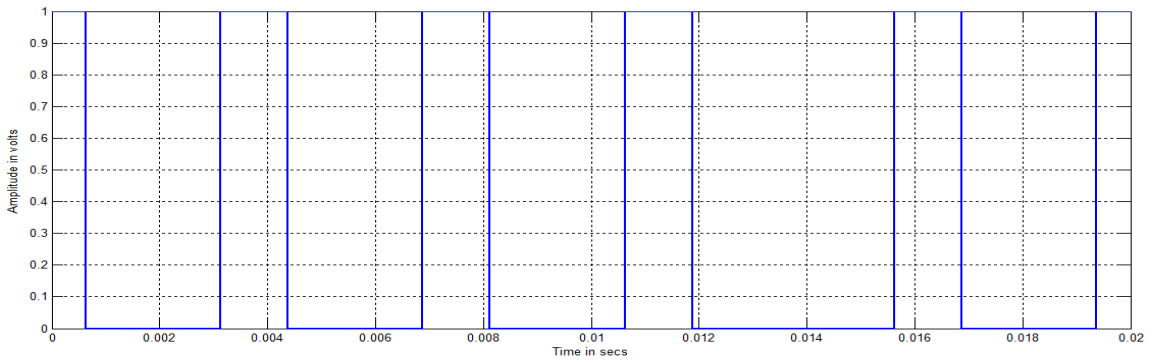

Figure 2. Gating pattern of Switch S11

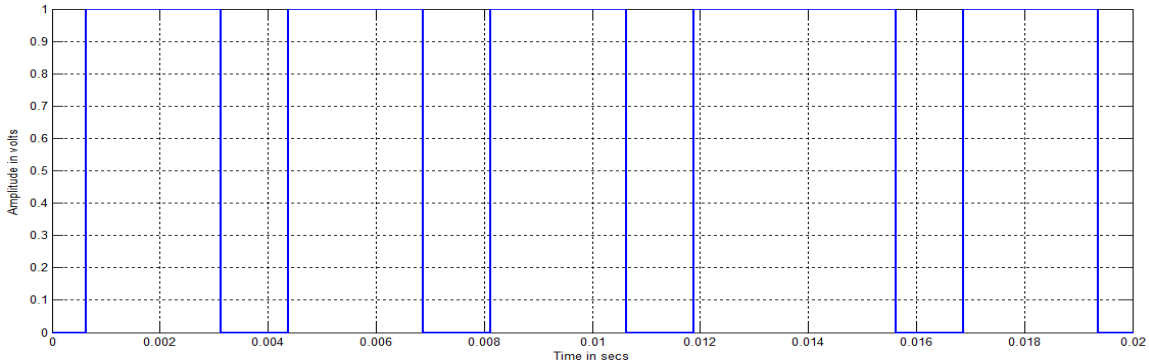

Figure 3. Gating pattern of Switch S12

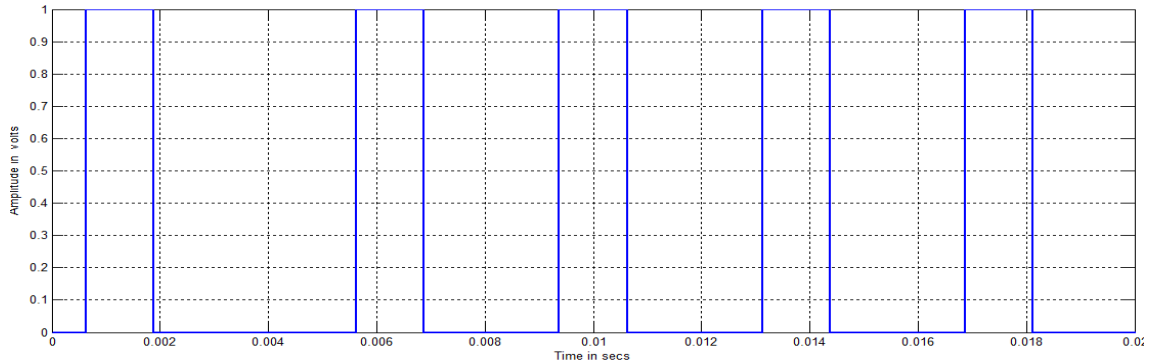

Figure 4. Gating pattern of Switch S13

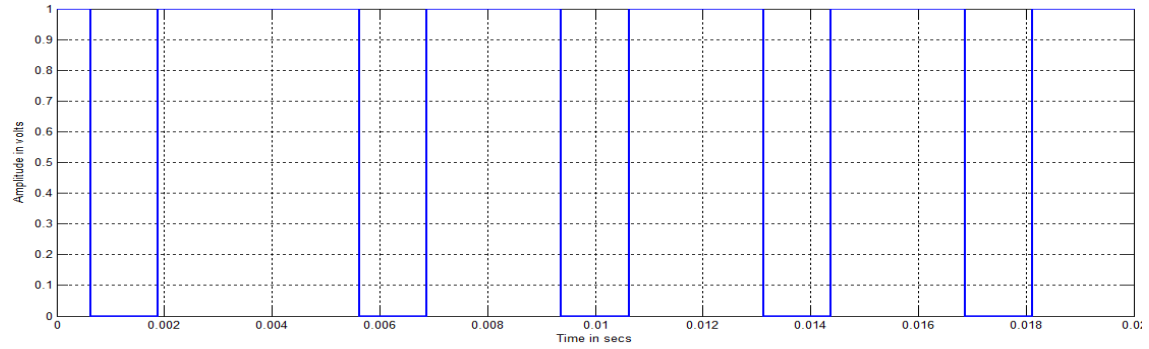

Figure 5. Gating pattern of Switch S14

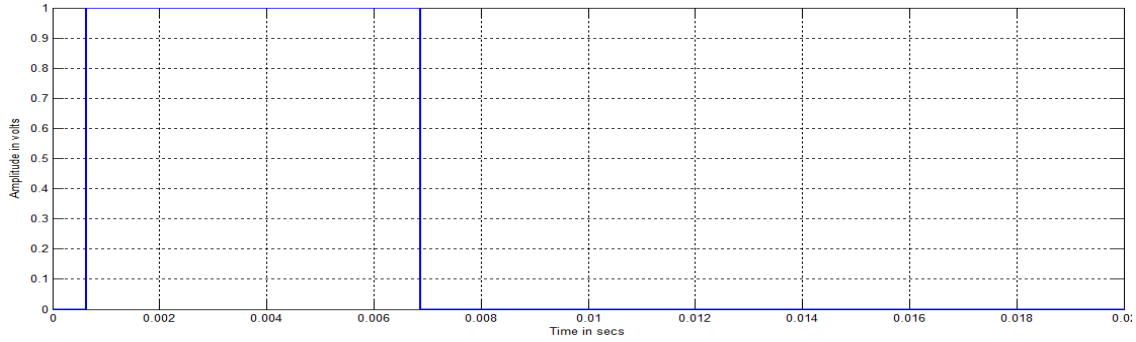

Figure 6. Gating pattern of Switch S21

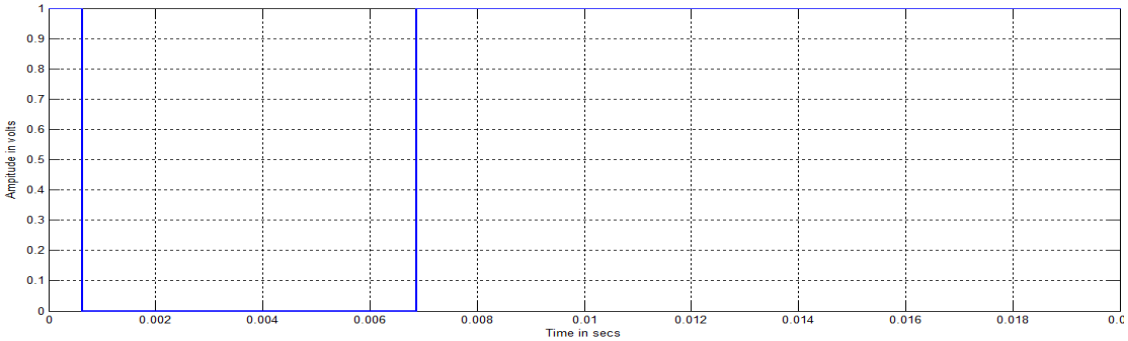

Figure 7. Gating pattern of Switch S22

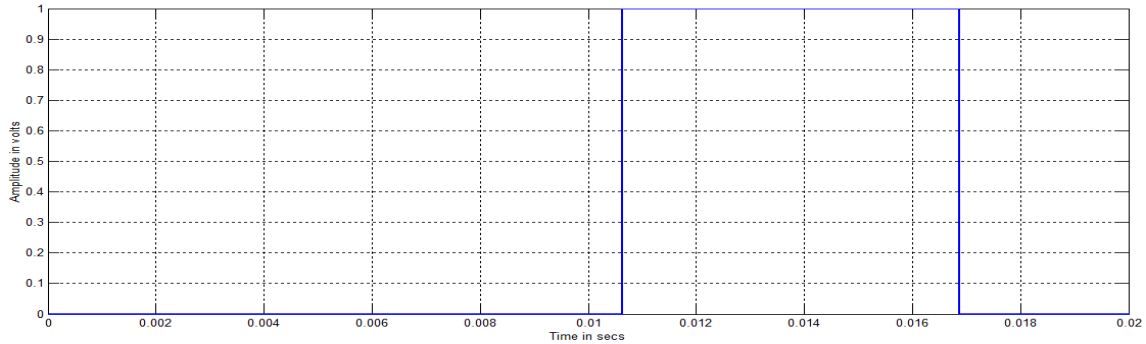

Figure 8. Gating pattern of Switch S23

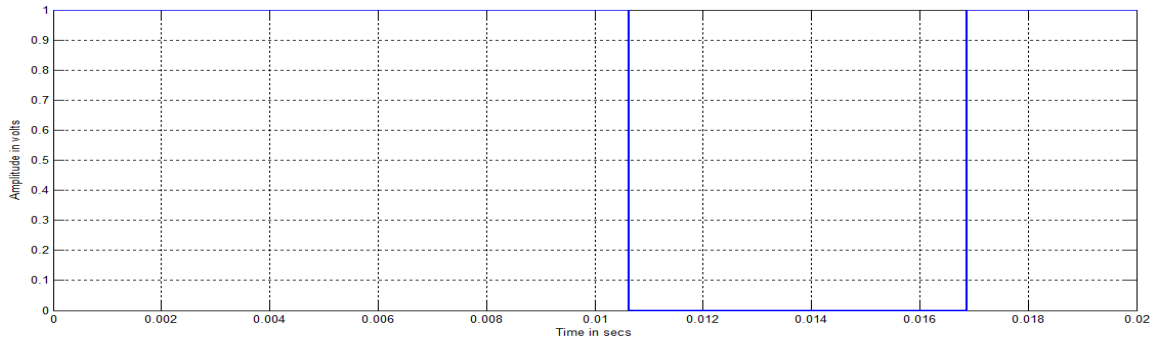

Figure 9. Gating pattern of Switch S24

3. SIMULATION RESULTS AND ANALYSIS

The Asymmetrical multilevel inverter was simulated using MATLAB. Figures 2-9 shows the gating pattern generated using embedded control technique Figures 10-12 shows simulation waveforms of upper inverter terminal voltage, lower inverter terminal voltage and nine level synthesised output voltage of trinary DC source inverter. Figure 13 shows the FFT plot for nine level inverter, where a THD of output voltage waveform is 14.9%. We can notice that the lower inverter generates a fundamental output voltage of three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Consequently the final output voltage becomes the sum of output voltage of upper and lower H bridge modules. The following parameter values are used for simulation: Vdc =25V, R (load)=100 ohms.

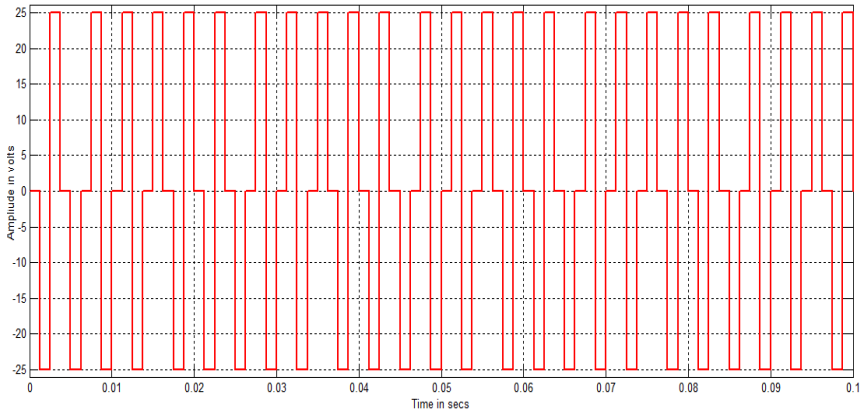

Figure 10. Upper inverter terminal voltage

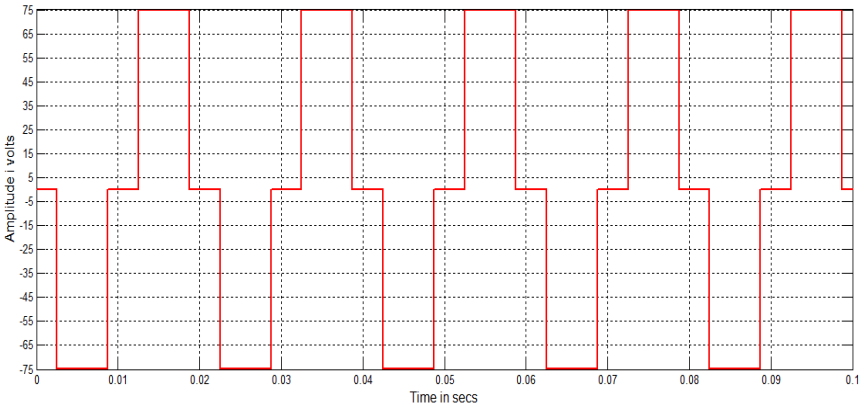

Figure 11. Lower inverter terminal voltage

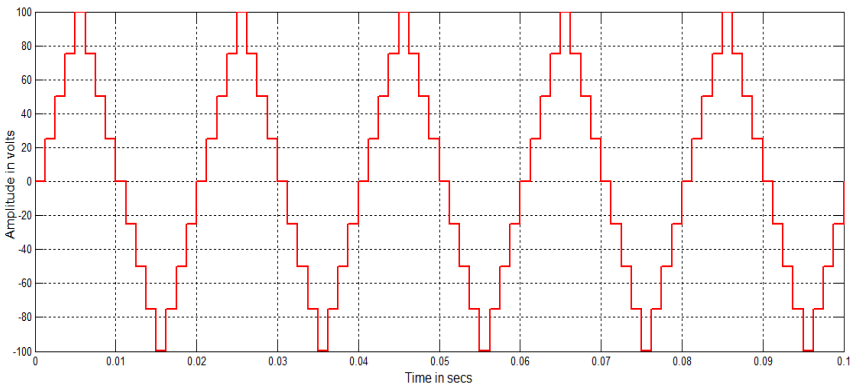

Figure 12. Nine level output voltage of AMLI

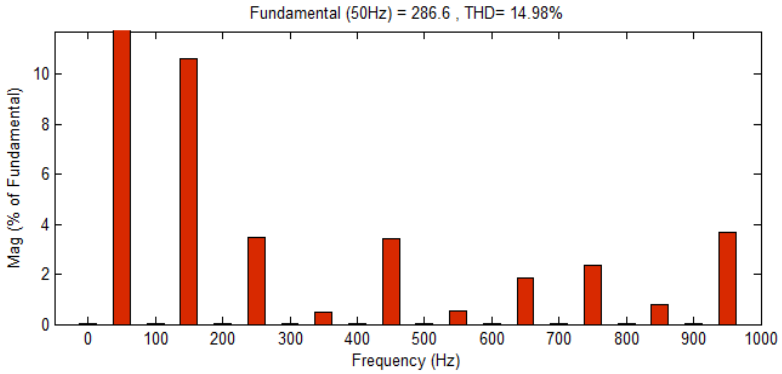

Figure 13. FFT plot for nine level output voltage

4. EXPERIMENTAL RESULTS AND ANALYSIS

The main part of the hardware circuit is the micro-controller. The line-interfacing unit gives the information about the supply to the microcontroller. A suitable program was written in the micro-controller to generate a train of pulses. In the control circuit, a 32 bit micro-controller was used. The driving pulse required for the MOSFETs IRF540 was obtained from microcontroller ARM Cortex™-M0 Core. It provides a highly flexible and cost effective solution to many embedded control applications. The MOSFETs (IRF540) were connected in the required fashion. For asymmetrical multilevel inverter, eight MOSFETs and two individual DC sources with ratio 1:3 are required. MOSFETs with anti-parallel diodes were employed as switching devices which is shown in Figure 14. The Figures 15-22 shows the switching pattern for the eight switches correspondingly. Figure 23 shows the output voltage waveform of a single phase cascaded H-bridge multilevel inverter. FFT analysis for nine level inverter is illustrated in Figure 24, where a THD of experimental output voltage waveform is 14.5%.

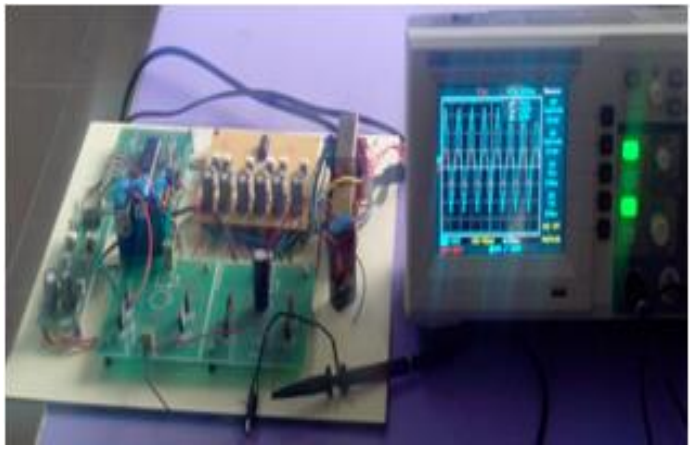

Figure 14. Prototype

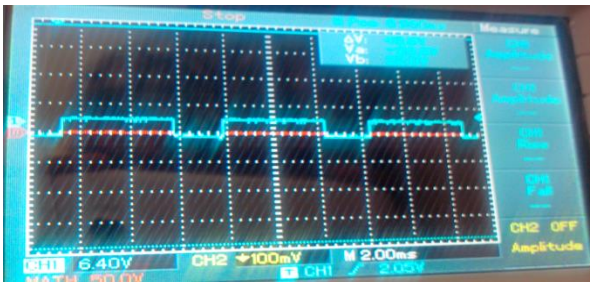

Figure 15. Gating pattern of Switch S11

Figure 16. Gating pattern of Switch S12

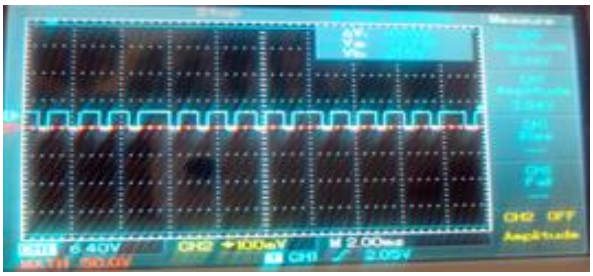

Figure 17. Gating pattern of Switch S13

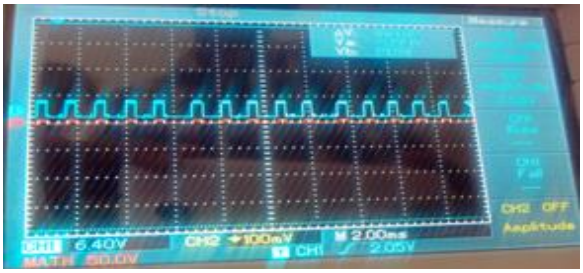

Figure 18. Gating pattern of Switch S14

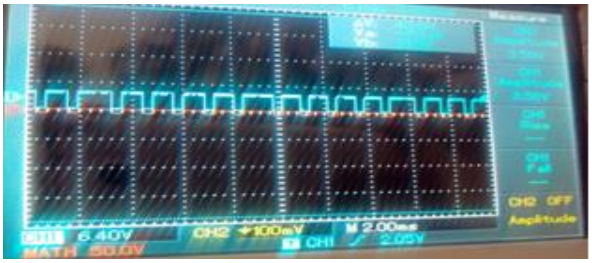

Figure 19. Gating pattern of Switch S21

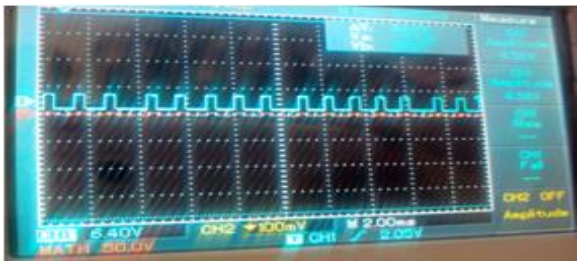

Figure 20. Gating pattern of Switch S22

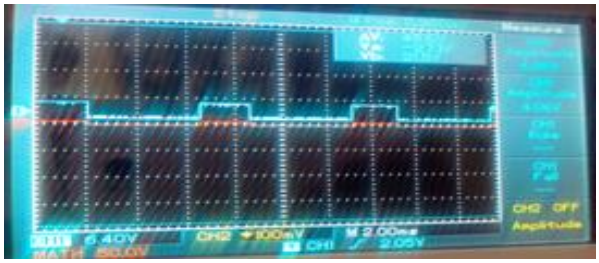

Figure 21. Gating pattern of Switch S23

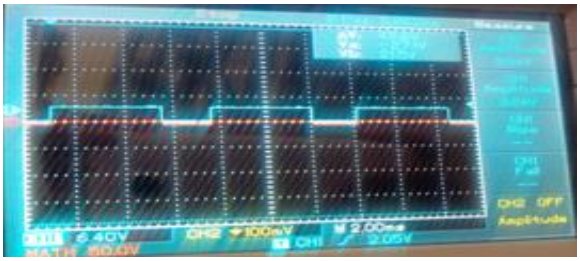

Figure 22. Gating pattern of Switch S24

Figure 23. Nine level output voltage of AMLI

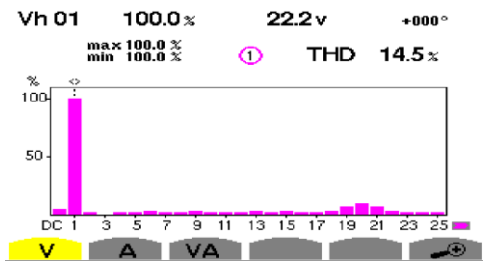

Figure 24. FFT plot for nine level output voltage

5. CONCLUSION

The symmetrical multilevel inverter with embedded controller are presented. The Asymmetrical multilevel inverter with 1:3 voltage propagation can produce high quality output voltage with less number of switches and voltage sources compare to conventional multilevel inverters. The proposed Switching scheme significantly reduces the Total Harmonic Distortion (THD) and reduces the complexity. The advantage of using embedded scheme is that it reduces the uneven degradation of power switches and switching losses. It is observed that proposed scheme produce THD in the range of 14%. This proposed system eliminates the complexity of generating gate signals when the stages are added.

REFERENCES

[1] Mariéthoz S., "Design and control of high-performance modular hybrid asymmetrical cascade multilevel inverters," *IEEE Trans. Ind. Appl*, 50(6):4018-4027, 2014.

[2] Mokhberdoran A, Ajami A. "Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology," *IEEE Trans. Power Electron*, 29(12):6712-6724, 2014.

[3] Arun V, Shanthi B, Arumugam M, "Analysis of Binary DC Source Reduced Switch 7-level Inverter," *International Journal Power Electron Drive Syst*, 6(1):70-76, 2015.

[4] Espinosa EE, Espinoza JR, Melín PE, et al. "A new modulation method for a 13-level asymmetric inverter toward minimum THD," *IEEE Trans. Ind. Appl*., 50(3):1924-1933, 2014.

[5] Manoharan MS, Ahmed A, Park JH. "A PV Power Conditioning System Using Asymmetric Multilevel Inverter with Hybrid Control Scheme and Reduced Leakage Current," *IEEE Trans. power Electron*, 32(10):7602-7614, 2017.

[6] Arun V, Shanthi B, Bharathi A, "Performance Evaluation of Various Unipolar SPWM Strategies of Trinary DC Source Multilevel Inverter," *International Journal of Engineering and Innovative Technology*, 2(6):458-462, 2012.

[7] Bharath R, Arun V, "9-Level Trinary DC Source Inverter Using Embedded Controller," *IOSR Journal of Engineering*, 2(10):90-95, 2012.

[8] Flores P, Dixon J, Ortuzar M, Carmi R, Barriuso P, Moran L, "Static Var Compensator and Active Power Filter With Power Injection Capability, Using 27-Level Inverters and Photovoltaic Cells," *IEEE Trans. Ind. Electron*., 56(1):130-138, 2009.

[9] Mekhilef S, Kadir MNA, Salam Z, "Digital Control of Three Phase Three-Stage Hybrid Multilevel Inverter," *IEEE Trans. Ind. Informatics*, 9(2):719-727, 2013.

[10] Arun V, Shanthi B, Natarajan SP. "Investigation of Digital Control Strategy for Trinary DC Source Cascaded Multilevel Inverter," *International Journal of Emerging Trends in Engineering and Development*, 1(3):382-390, 2013.

[11] Mortezaei A, Simoes MG, Bubshait AS, Busarello C, Marafao FP, Al-Durra A., "Multifunctional Control Strategy for Asymmetrical Cascaded H-Bridge Inverter in Microgrid Applications," *IEEE Trans. Ind. App.*, 53(2):1538-1551, 2017.

[12] Devaraj N, Reena A, "Reduction of switches and DC sources in Cascaded Multilevel inverter," *Bulletin of Electrical Engineering and Informatics (BEEI)*, 4(3): 186-195, 2015.