Switching regulator based on an adaptive DC-DC buck converter for a lithium-ion battery charging interface

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Article Info

ABSTRACT

A switching regulator based on an adaptive DC-DC buck converter for a Li-ion battery charging interface is introduced in this paper with the aim of improving the efficiency of charging the Li-ion battery during the whole charging process. By using the battery voltage as feedback, an adaptive reference is generated. This reference is employed by the converter, which is in continuous conduction mode (CCM), to produce a wide adaptive output voltage that closely tracks the battery voltage, intended to serve as the power source for the multimode charging interface. The converter was implemented in a 180 nm complementary metal oxide semiconductor (CMOS) process and simulated using the Cadence Virtuoso tool. With an input voltage of 5 V and a switching frequency selected at 500 kHz, the simulation results show that the converter produces different charging currents for each battery charging mode, and an adaptive output voltage ranging from 2.8 V to 4.38 V, with the current ripple of 38 mA in CC mode and voltage ripple factor less than 1% in constant voltage (CV) mode. The average converter efficiency is 83.5%.

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1. INTRODUCTION

With the growing demand for mobile applications, portable electronic devices have become an integral part of our daily lives. One of the key components that power these devices is the Lithium-Ion batteries (LIBs) because they offer significant advantages over other battery technologies: remarkable energy density making them the ideal choice for these devices where space is limited, extended cycle life for sustained usage (greater than 1000 cycles), immunity to memory effect, and a low self-discharge rate (2% to 8% per month). Moreover, a LIB cell can operate within a wide range from 2.5 V to 4.2 V with a nominal voltage of 3.6 V [1]–[4].

However, LIBs are irreversibly degraded by overcharge or over-discharge, requiring the selection of appropriate charging protocols and strategies [5], [6]. One of the most widely used strategies for charging these batteries is constant current-constant voltage (CC-CV) charging due to its simplicity of implementation and battery prevention [7], [8]. As depicted in Figure 1, this strategy can be composed of three charging modes: Pre-charge mode, constant current mode (CC mode), and constant voltage mode (CV mode). The first mode is needed when the battery is deeply discharged and its voltage is below a threshold voltage V_{th}. In this case, a low current, known as the trickle current, is applied to precondition the battery for normal charging. When the battery voltage exceeds the V_{th} threshold, the charging protocol switches to CC charging mode. During this phase, the battery is charged with a large current, while its voltage rises rapidly until it

approaches a V_{full} voltage regulation limit. Once the battery voltage reaches this limit, the CV charging mode begins. In this mode, the battery voltage is kept constant, and the charging current decreases until a predefined termination current is reached, at which point the battery charging is stopped.
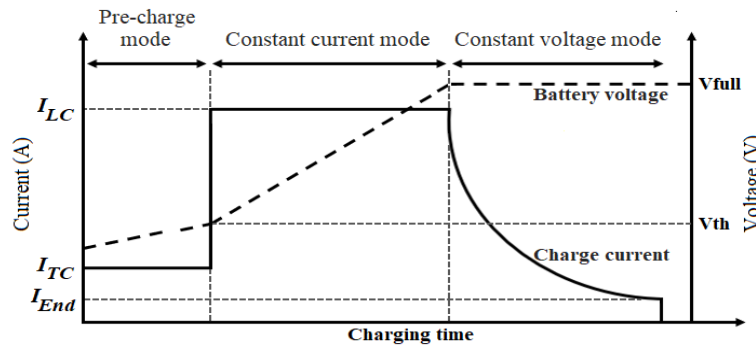

Figure 1. Typical Li-ion battery charging strategy

Various integrated circuit architectures using this charging strategy have been developed to charge LIBs. These architectures are generally grouped into two families: Linear chargers based on a low-dropout regulator (LDO) and switching-based chargers. The linear charger presents the advantages of complete on-chip integration, compact size and high accuracy. Its typical block diagram is illustrated in Figure 2(a); Most linear chargers are designed to operate with a fixed supply voltage [9]–[11]. However, these chargers suffer from reduced efficiency due to the large deviation between the input supply voltage and the battery voltage. Indeed, Figure 2(b) shows that the difference between the supply voltage and the battery voltage is considerable at the beginning of charging process, particularly when the battery voltage V_{bat} is small, which will increase power dissipation and therefore impact charger efficiency.
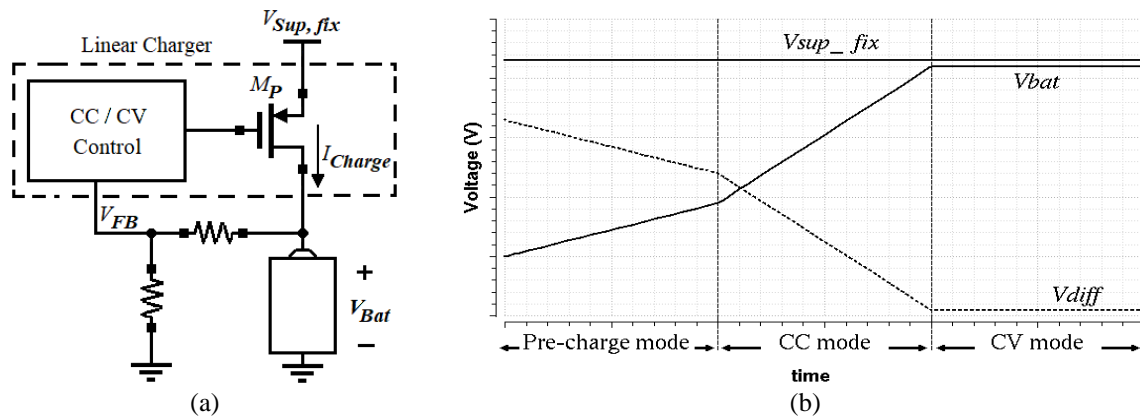

Figure 2. Linear charger (a) with fixed supply voltage and (b) waveform of the deviation between V_{Sup_fix} and V_{bat}

To ensure high charging efficiency for LIBs, switching charger ICs are implemented in [12]–[14]. Architectures [12] and [13] mention the buck converter-based structure. However, the pre-charge mode is not introduced, which can damage the battery or affect its lifespan by applying a large current at the start of the charging process. A controller with a transformer fly-back topology presented in [14] achieves high efficiency but increases the size of the charging circuit.

In order to make efficient use of the energy available from the power source to charge the LIB and minimize power dissipation, we introduce in this paper a DC-DC buck converter. The converter is in continuous conduction mode (CCM) and produces an adaptive voltage that closely tracks the battery voltage and will be used as a voltage source for a multimode Li-ion battery charging interface (BCI) presented in [15]. This paper uses the battery model, represented by the first-order Thevenin equivalent circuit as discussed in [16]–[18]. The

rest of this paper is structured as follows: Section 2 includes the description, analysis and implementation of the circuit. Simulation results are presented and discussed in section 3, and section 4 concludes the paper.

2.   CIRCUIT ANALYSIS AND IMPLEMENTATION

The block diagram of the adaptive DC-DC buck converter with the multimode Li-ion battery charging interface is shown in Figure 3. It includes three fundamental blocks: a power stage, a control stage and the multimode BCI. Based on the battery voltage information V_{bat}, two diode-connected PMOS transistors (MP1, MP2) and a level shifter generate an adaptive reference signal V_{ad-ref}, which is compared in the compensator to a fraction of the converter output voltage V_{fb} extracted via a voltage divider formed by resistors R_{fb1} and R_{fb2} (1). The resulting error V_{comp} is first amplified and compensated and then applied to the non-inverting input of a pulse width modulation (PWM) comparator. Via a ramp generator, a sawtooth signal V_{ramp} is generated and applied to the inverting input of the comparator. The comparison between V_{comp} and V_{ramp} results in a PWM signal V_{pwm} with a varying duty cycle.

$$V_{fb} = \frac{R_{fb2}}{R_{fb1}+R_{fb2}} V_0 \qquad (1)$$

Once the V_{pwm} signal is available, it is applied to the non-overlap circuit. This circuit will then produce the two dephased signals V_{P1} and V_{N1}, which are applied to the driver section, then to the high-side and low-side switches (HSS and LSS). To complete the circuit diagram, a multimode BCI presented in [15] is used as a load for the converter. Finally, depending on the battery's state of charge, the converter adjusts its output voltage to track the battery voltage more closely.
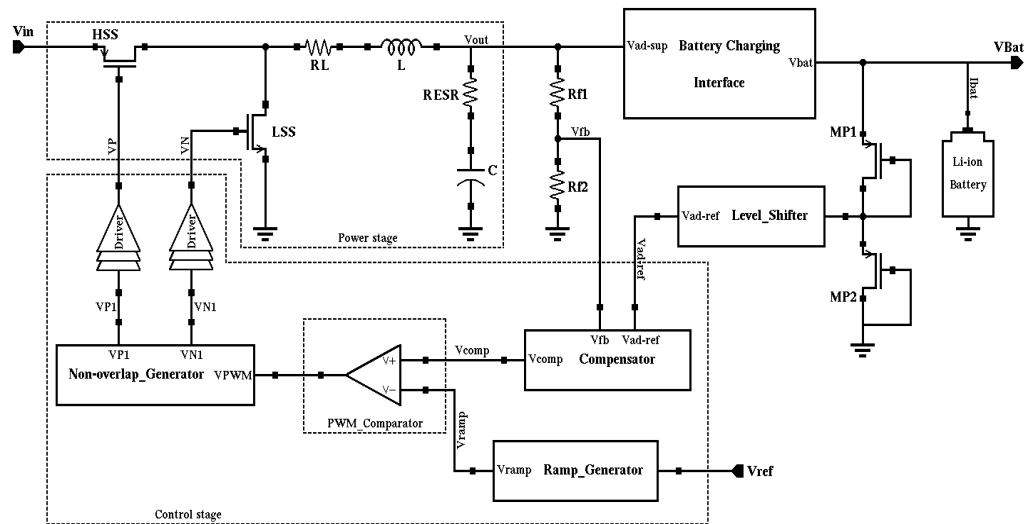

Figure 3. Block diagram of adaptive buck converter with BCI

2.1. Power stage

The power stage consists of HSS and LSS switching elements and an LC filter. This stage converts the input voltage V_{in} to the desired output voltage. The appropriate dimensioning of inductance L and capacitance C is determined using the mathematical model of a conventional buck converter [19]–[21]. In addition, the values of L and C have been chosen to ensure that the current and voltage requirements of the BCI are satisfied. These values are set at $16\ \mu H$ ($R_L = 35\ m\Omega$) and $21\ \mu F$ ($R_{ESR} = 5\ m\Omega$) respectively. The LC filter can be described as a second-order system. Its transfer function has a double pole at frequency $F_{LC} = 8.7\ kHz$, and a zero at frequency $F_{ESR} = 1.5\ MHz$ generated by the equivalent series resistor R_{ESR}.

2.2. Control stage

Based on the adaptive reference voltage V_{ad-ref}, the control stage supervises the switching operation by adjusting the duty cycle to regulate the converter output voltage. Due to its simplicity and high noise immunity, the control scheme adopted is the voltage-mode PWM scheme described in [22], [23]. The

control stage includes the following circuits: Compensator, PWM comparator, ramp generator and non-overlap with gate driver circuit.

2.2.1. Compensator

The LC filter introduces a pair of poles into the system's feedback loop, causing phase degradation and therefore, the converter can easily become unstable. To improve the phase margin and make the converter unconditionally stable, a compensation circuit is required. Figure 4(a) shows the schematic diagram of the type 3 compensation circuit used. Its transfer function has one pole at the origin f_{p0} and two pairs (zero-pole) at the frequencies (f_{z1}, f_{p1}) and (f_{z2}, f_{p2}) respectively. The corresponding equations are obtained by (2) and (3).

$$H(s) = \frac{R_{fb1} + R_3}{R_{fb1}R_3C_1} \frac{1}{s} \frac{\left(s + \frac{1}{R_2C_2}\right)\left(s + \frac{1}{(R_{fb1}+R_3)C_3}\right)}{\left(s + \frac{1}{R_3C_3}\right)\left(s + \frac{C_1+C_2}{R_2C_1C_2}\right)} \tag{2}$$

$$f_{z1} = \frac{1}{2\pi R_2 C_2} , \quad f_{z2} = \frac{1}{2\pi (R_{fb1} + R_3)C_3}$$

$$f_{p0} = 0 , \quad f_{p1} = \frac{1}{2\pi R_3 C_3} , \quad f_{p2} = \frac{C_1 + C_2}{2\pi R_2 C_1 C_2} \tag{3}$$

The values of the compensator's capacitive and resistive components are listed in Table 1. In Figure 4(b), the Bode diagram of the converter is displayed for $V_{out} = 4\,V$ and $I_{load} = 986\,mA$. It is worth noting that the phase margin is $51\,deg$ and the gain margin is $29\,dB$.

Table 1. Compensator parameters

Compensator components	Value
Capacitor C_1	$3.1\,pF$
Capacitor C_2	$1.1\,nF$
Capacitor C_3	$3.5\,nF$
Resistor R_{fb1}	$6.5\,k\Omega$
Resistor R_{fb2}	$5\,k\Omega$
Resistor R_2	$34.5\,k\Omega$
Resistor R_3	$180\,\Omega$

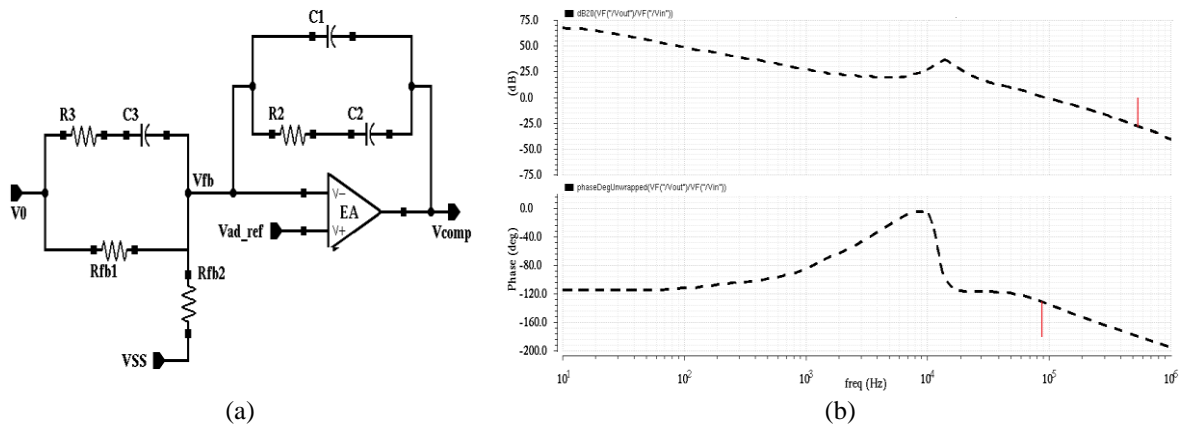(a)   (b)

Figure 4. Implementation of type 3 compensation: (a) circuit diagram and (b) bode plot of the voltage loop gain of the converter for $V_{out} = 4\,V$ and $I_{load} = 986\,mA$
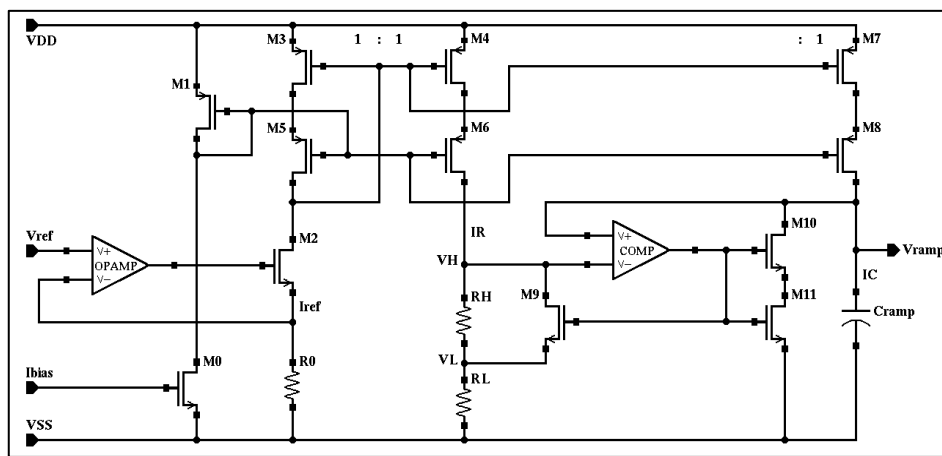
2.2.2. Ramp generator

Figure 5(a) illustrates the ramp generator circuit used to generate the sawtooth signal. In this circuit, a negative feedback loop established, by the operational amplifier OPAMP and transistor M2, produces a current I_{ref} flowing through resistor R_0. I_{ref} is controlled by the voltage V_{ref} delivered by a bandgap [24] (4). From I_{ref}, I_R and I_C currents are mirrored via a cascode current mirror. The I_R current flowing through resistors R_L and R_H in series provides the two threshold voltages V_L and V_H. Finally, the V_{ramp} voltage is generated by charging and discharging the C_{ramp} capacitor. Depending on the state of transistor M9, which is controlled by

the COMP comparator output voltage, the comparator's inverting input can be connected to either V_L or V_H. When transistors M9–M11 are off, the inverting input of the COMP is connected to V_H and the I_C current charges the capacitor. During this phase, the V_{ramp} voltage increases linearly until it reaches V_H. At this point, the comparator output switches, activating transistors M9–M11; making the COMP's inverting input connected to V_L this time. In this case, the capacitor will discharge and the V_{ramp} voltage will drop rapidly to V_L. At this value, the COMP output switches, returning transistors M9–M11 to the off state, and a new cycle begins.

Due to the rapid discharge of the capacitor, the V_{ramp} period is almost equal to the charging time. This period is expressed by (5). The simulation result for the ramp generator is shown in Figure 5(b). The resulting signal waveform is a periodic ramp with a maximum of 2.6 V and a minimum of 0.7 V. The signal frequency is 500 kHz.

$$I_{ref} = \frac{V_{ref}}{R_0} \tag{4}$$

$$T_{ramp} = \frac{(V_H - V_L)}{I_C} C_{ramp} = \frac{R_H I_R}{I_C} C_{ramp} = R_H C_{ramp} \tag{5}$$

(a)
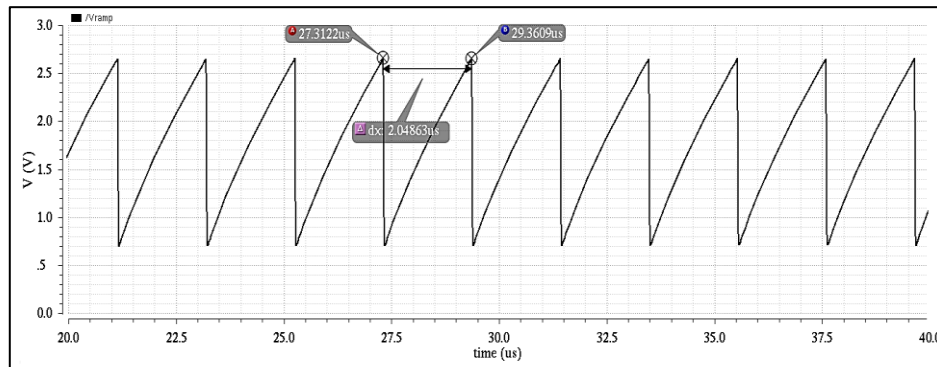
(b)

Figure 5. Ramp generator (a) circuit diagram and (b) waveform of ramp signal

2.2.3. Non-overlap generator and gate driver circuit

The signals intended to control the HSS and LSS switches must be generated so that these two transistors operate in a complementary manner. To achieve this, a delay (dead time) is introduced to avoid simultaneous current conduction in both power transistors, and thus prevent a short-circuit path from supply to ground. This operation is performed by the non-overlap generator shown in Figure 6(a). On the other hand, the considerable size of power transistors makes their gate capacitance excessive and difficult to drive. Consequently, the implementation of a gate driver circuit is required [25]. Figure 6(b) shows the gate driver schematic, which comprises four simple inverter stages. The transistors in each stage are sized by a constant factor (called taper factor) relative to the transistors in the previous stage. The non-overlapping V_P and V_N waveforms controlling the switches are depicted in Figure 6(c).
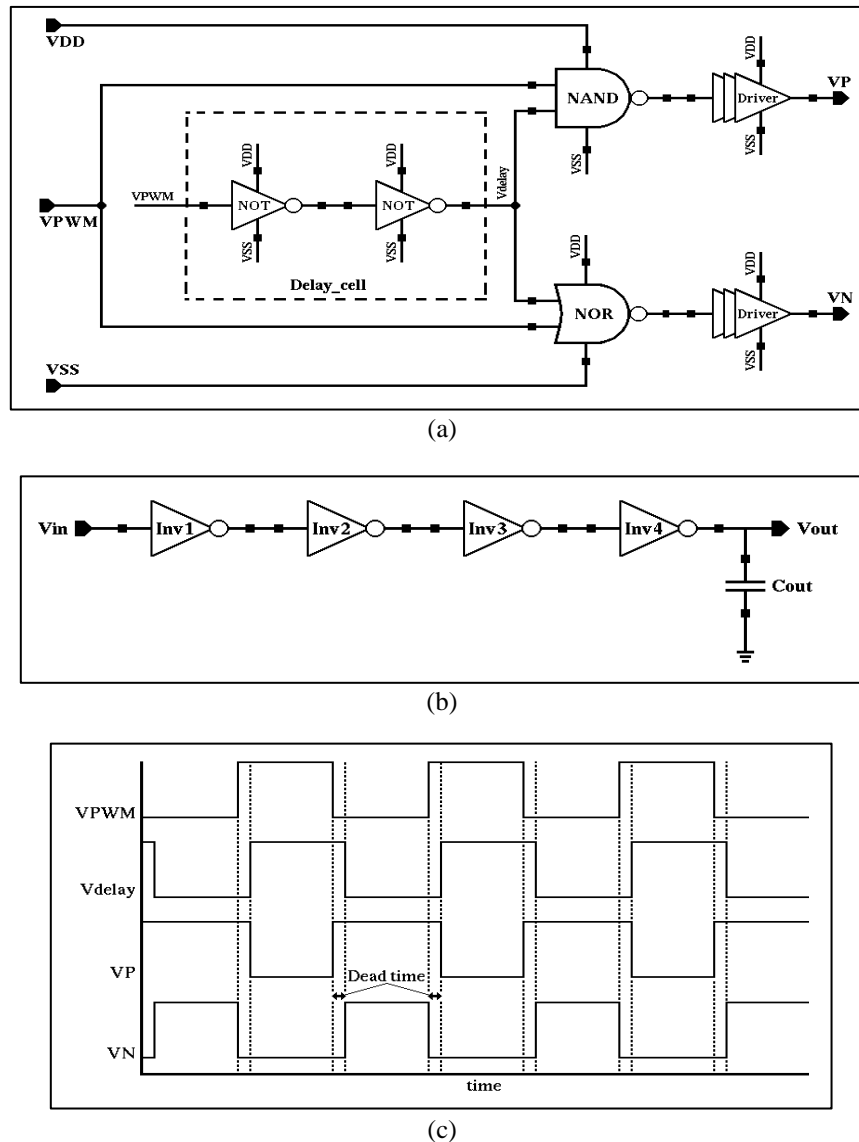
(a)

(b)

(c)

Figure 6. Non-overlapping generator and gate driver (a) non-overlap, (b) driver circuit, and
(c) non-overlapping signal waveforms and dead time

3. RESULTS AND DISCUSSION

To evaluate the effectiveness of the proposed converter in generating an adaptive voltage suitable for our Li-ion BCI and to confirm that it meets the required specifications, a simulation was performed using the Analog Design Environment tool in Cadence Virtuoso software. The first-order Thevenin model for the battery in this simulation includes a capacitance with an equivalent parallel resistance of $(1\ mF, 5\Omega)$ and an internal resistance of $250\ m\Omega$.

Figure 7 shows the temporal evolution of V_{out} and V_{bat}, demonstrating that the converter produces an extended adaptive output voltage varying from 2.8 V to 4.38 V, which closely follows the battery voltage with a certain deviation. It is remarkable that this deviation gradually decreases as the battery is charged. According to Figure 8, the output voltage ripple in CV mode is $874\ uV$, which represents less than 1%.

Figure 9(a) illustrates the inductance current variations as a function of time, and shows that the converter generates the three charge currents required for BCI operation. During the pre-charge mode, it is observed that the average charge current is $183\ mA$. As shown in Figure 9(b), when the BCI operation switches to CC mode, the current rises to an average value of $986\ mA\ (\approx 1\ A)$, with a current ripple of approximately $38\ mA$. When the BCI operates in CV mode, the inductance current reaches a value of $80\ mA$ at the output voltage of 4.38 V. Furthermore, the converter maintains its operation in continuous conduction mode across all three charge modes.
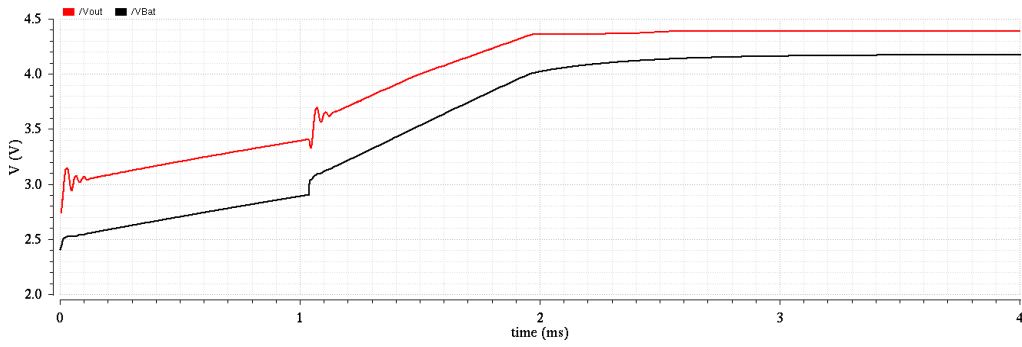
Figure 7. Simulation results of converter output voltage and battery voltage
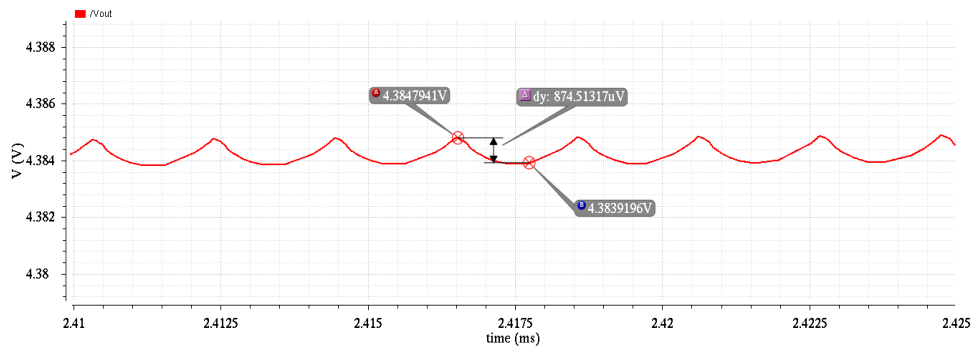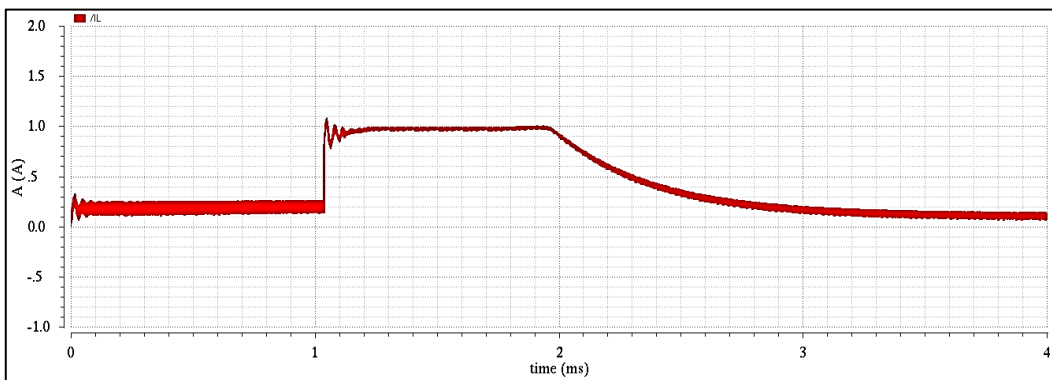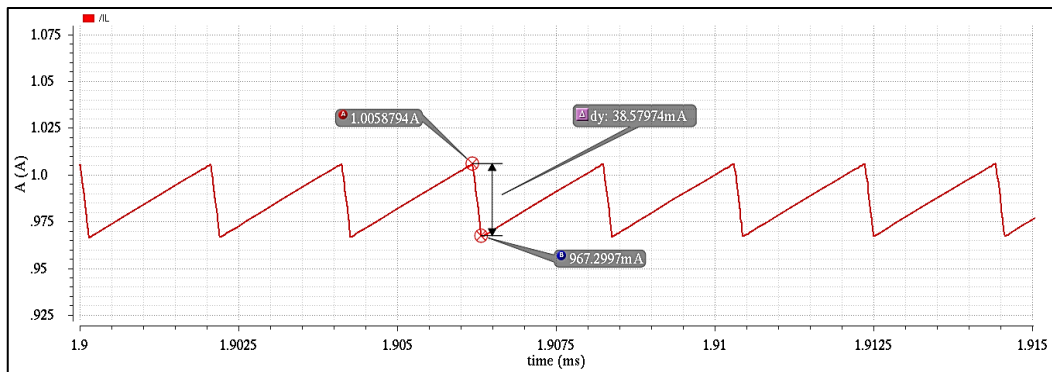

Figure 8. Ripple measurement result of converter output voltage in CV mode

(a)

(b)

Figure 9. Inductance current simulation result (a) inductance current variation and (b) measurement of inductance current ripple in CC mode

As previously mentioned, the deviation between the adaptive voltage generated by the converter and the battery voltage gradually decreases during the charging process, leading to an enhancement in the overall system efficiency. This can be seen in Figure 10, which shows the variation in converter efficiency as a function of output voltage. According to this figure, the efficiency reaches its maximum of 97.8% when the output voltage is 4.26 V. The average efficiency of the converter is 83.5%.

Finally, Figure 11 gives the variations of V_{bat} and I_{bat} provided by the BCI allowing the reconstruction of the charging diagram of a LIB, and it demonstrates that the designed buck converter fully satisfies the current and voltage criteria of the charging interface.
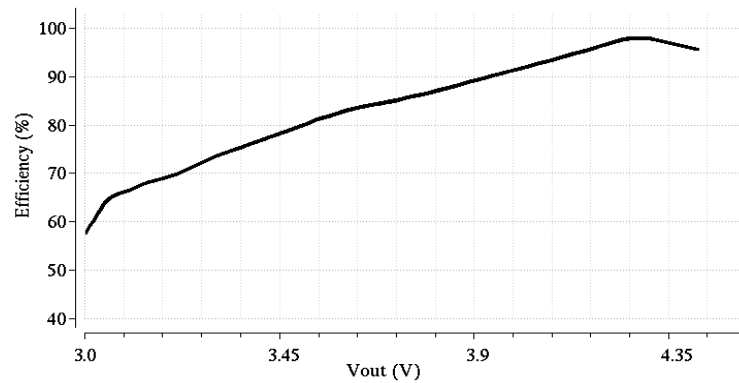
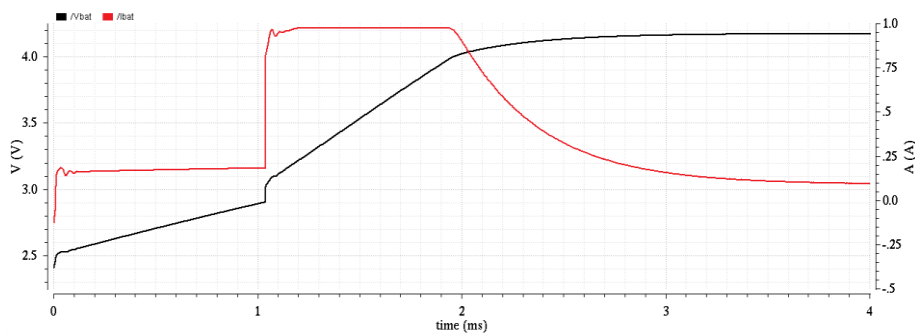Figure 10. Converter power efficiency as a function of output voltage

Figure 11. Simulation result of LIB charging diagram

4.   CONCLUSION

In this paper, a detailed design of a DC-DC buck converter operating in continuous conduction mode has been presented. The converter is specifically designed to generate an adaptive output voltage, intended as a power source for a Li-ion battery charging interface. The implementation is realized in a 180 nm complementary metal oxide semiconductor (CMOS) process. Simulations are performed in Cadence Virtuoso to evaluate the converter performance. The study covers the description of the conceptual idea and the analysis and implementation of the circuit components. The results obtained demonstrate that the converter has the ability to provide an adaptive voltage ranging from 2.8 V to 4.38 V. Average power efficiency is 83.5%, offering a robust energy solution in advanced CMOS environments. This approach offers significant contributions to the design of DC-DC converters for specific Li-ion battery applications, with potential implications for embedded systems and battery-powered electronic devices.

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