IAES International Journal of Robotics and Automation (IJRA)
Vol. 14, No. 4, December 2025, pp. 459~467
ISSN: 2722-2586, DOI: 10.11591/ijra.v14i4.pp459-467

Design of low-power, high-speed approximate 4:2 compressors for efficient partial product reduction in multipliers

Jabez Daniel Vincent David Michael[1], Anusha Gorantla[2], Ahilan Appathurai[3], Dinesh Ramachandran[4]
[1]Department of Electronics and Communication Engineering, Dr. Sivanthi Aditanar College of Engineering, Thiruchendur, India
[2]Department of Electronics and Communication Engineering, Raghu Engineering College, Visakhapatnam, India
[3]Department of Electronics and Communication Engineering, PSN College of Engineering and Technology, Tirunelveli, India
[4]Information Science and Engineering, HKBK College of Engineering, Bangalore, Karnataka, India

Article Info

Article history:

Received Oct 3, 2024
Revised Nov 1, 2025
Accepted Nov 11, 2025

Keywords:

Approximate computing
Compressor
Delay
Low power
Multiplier
Partial product reduction

ABSTRACT

Partial product reduction becomes the main task in the multiplication process. Therefore, the partial product stages of multipliers are reduced with the usage of compressors, by using compressors in the multiplier. Using compressors in the multiplier circuit significantly impacts multiplier performance. Approximate compressors are crucial for achieving better design metrics in parallel multipliers. This paper proposes to create various new approximate 4:2 compressor circuits. A trade-off is made between the performance and accuracy of this approximate circuit design approach. The proposed designs have been implemented using XOR-XNOR gates with a 2-to-1 multiplexer, and also XOR-XNOR gates with transmission gates. All these circuits have been simulated using Cadence in different technological nodes. Compared with the existing technique, the proposed 4:2 approximation compressor provides 51.4% power reduction and 26.45% delay reduction for 45 nm equipment.

Corresponding Author:

Anusha Gorantla
Department of Electronics and Communication Engineering, Raghu Engineering College
Visakhapatnam, Andhra Pradesh 531162, India
Email: anushagorantla3@gmail.com

1. INTRODUCTION

Low energy usage is a significant problem when designing efficient computing systems in approximate computing [1]. This strategy can improve efficiency [2] without sacrificing acceptable quality by using approximate computations [3]. Approximate computing is more suitable in embedded and mobile systems [4] and also in image recognition, data mining, and machine learning [5]. There are several VLSI abstractions [6], including the algorithmic, architectural, logic, gate, and transistor levels [7].

During multiplication, the partial product reduction stage has high power consumption [8], large silicon area, and more delay due to repeated additions [9]. Therefore, compressors are used to improve the circuit performance [10]. In a 4-2 compressor design, the transistor count ranges from 40 to 28 [11]. The XOR makes use of a 6T XOR-XNOR gate [12]. The adders considered approximate implementation in the lower partial OR adder [13]. In approximations, a one-bit adder, or full adder, and the circuit is built using basic gates [14]. Inverters, two-input NAND, NOR, XOR, and XNOR are examples of basic gates used to calculate [15].

Gate-level logic complication reductions are proposed by the author to reduce the logic complexity [16]. A similar kind of 4:2 compressors found a comparative evaluation of four different approximate adders [17]. The purpose of the approximate compressor is presented for biomedical applications [18].

Recently, a variety of compressors have been proposed to reduce delay while performing repeated tasks [19], and these were employed in multipliers to accord configurable multipliers [20]. Approximate multipliers [21] for distinct columns are synthesized using the 28nm technology [22]. Simulations are conducted on the component and utilization layers to evaluate outcomes [23]. Compressors lower precision and enter the domain of approximation computing by evaluating [24]. An unsigned approximation multiplier design enhances hardware efficiency without losing precision [25]. A unique 4:2 approximation compressor is used to simplify the product's intermediate sections [26], and the incorrect result. The majority of multipliers are generated with reasoning; determining would result in considerable inaccuracy [27].

From the recent research, the existing techniques face challenges like more delay, power consumption, and more area occupation. Traditional multipliers suffer from high power usage, large silicon area, and delay, are affect the speed of hardware. To address these issues, approximately 4:2 compressors were developed. The proposed method reduces the usage of transistor count and lowers the complexity. The proposed compressor achieves low power consumption and delay at 6T XOR-XNOR gates and 2T Multiplexer. The proposed approximate compressor is error-tolerant and energy-efficient. The result accuracy has been confirmed by metrics such as MRED and NMED.

The research questions for the proposed method are how the approximate 4:2 compressor significantly reduces power usage and delays, and how the 4:2 compressor enhances efficiency and speed performance. A detailed discussion on the existing 4:2 compressors is presented in Section 2, while Section 3 describes the design method for the organized 4:2 compressor. Section 4 offers a comparative analysis of existing and organized designs, and Section 5 concludes the paper.

2. EXISTING METHOD

In general, a multiplier uses a compressor to cut down on the stages of partial production. The compressor 4-2 [2] includes 5 inputs and three outputs. Figure 1 shows a 4:2 compressor. Therefore output equations of the exact 4:2 compressor are given by

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{in} \quad (1)$$

$$Carry = X_4(X_1 \oplus X_2 \oplus X_3 \oplus X_4) + Cin\,(X_1 \oplus X_2 \oplus X_3 \oplus X_4) \quad (2)$$

$$Cout = X_3(X_1 \oplus X_2) + X_1(X_1 \oplus X_2) \quad (3)$$

The 4-2 architectures using XOR-XNOR gates with 2 to 1 multiplexer and XOR-XNOR gates with transmission gates. The sum expression in terms of two input XOR-XNOR gates is as follows.

$$Sum = C_{in}[(X_1 \oplus X_2)(X_3 \oplus X_4)' + ([(X_1 \oplus X_2)'(X_3 \oplus X_4)]' + C_{in}'[((X_1 \oplus X_2)(X_3 \oplus X_4)' + (X_3 + X_4)] \quad (4)$$

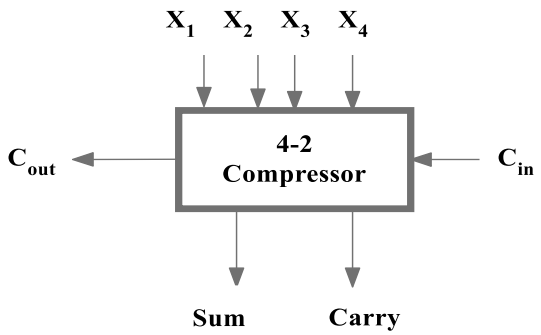

Figure 1. 4:2 compressors

3. PROPOSED APPROXIMATE 4:2 COMPRESSORS

Our cutting-edge approximation reduces each of the five inputs and three outputs to four inputs and two outputs before grounding one of the four inputs with a 4-2 compressor. In our proposed design, approximations were made considering truth tables and Boolean expressions for precise 4-2 compressor carry

and output sum. From Table 1, we can see that the eight upper binary bits of X_4 and C_{in} are equal compared to the other lower inputs (X_3, X_2, and X_1). Therefore, we are approximating, X_4=C_{in}, and in the output columns, as there were two carry outputs, namely Carry and C_{out}, they are combined as Cout. When X_4=C_{in} and Carry= C_{out}, consists of the 5-input and 3 outputs of 4-2 compressor is reduced to 4 inputs and 2 outputs, respectively. Table 1 displays the Truth Table (TT) for the proposed approximate 4-2 compressor.

Table 1. TT of approximate 4:2 Compressor2

X4	X3	X2	X1	Carry	Sum
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	1

If all 1's of X_4 are replaced with '0' in Table 2, the last eight rows of inputs, Carry and Sum columns are a replication of the first eight rows, hence neglecting the last eight rows in Table 1, the logic here is inspected as a Full adder with grounded X4 input as laid out in Figure 2.

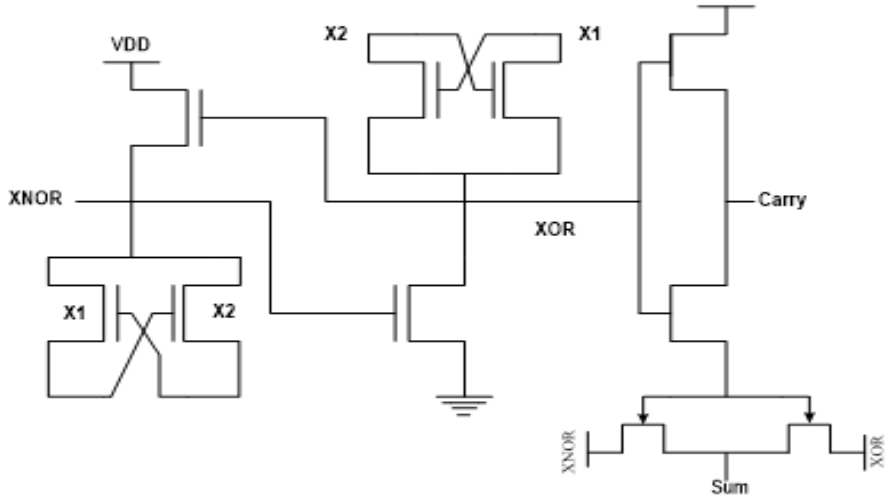

Figure 2. Gate level structure of the proposed 4:2 compressor

Considering (1) and equalizing X_4 and C_{in},

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus X_5 \quad (5)$$

$$Sum = X_1 \oplus X_2 \oplus X3 \quad (6)$$

From (5), X_4 XOR X_4 is zero, which reduces it to (6), now if all 1's of X_4 is replaced with '0' in Table 2, the last eight rows of inputs, Carry and Sum columns are replication of the first eight rows, hence neglecting the last eight rows in Table 2, the logic here is inspected as a Full adder with grounded X_4 input as laid out in Figure 3.

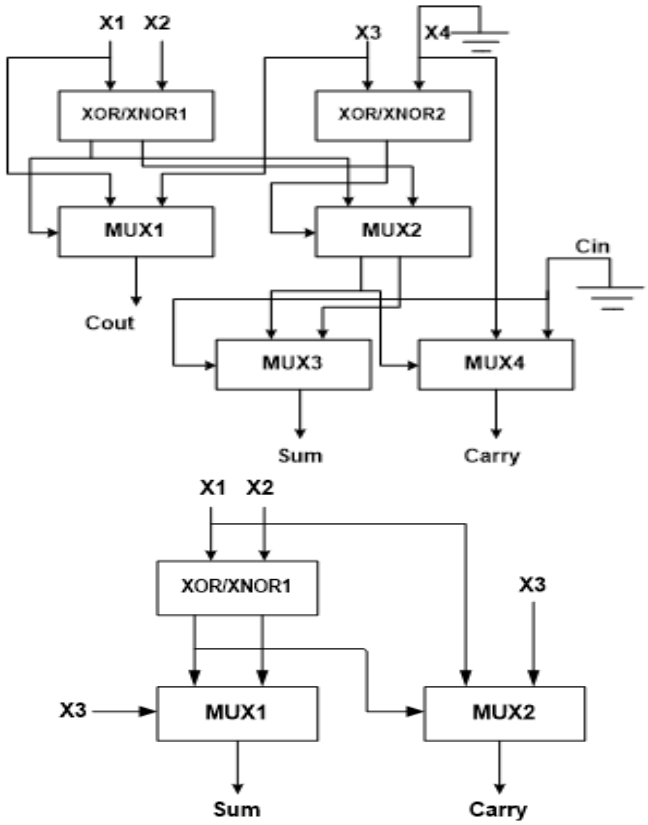

Figure 3. Block diagram of proposed approximate 4:2 compressor2

A condensed representation of the Figure 3 block diagram. A proposed compressor's Table 2 is shown in Figure 3, in which XOR-XNOR and MUX blocks are executed with 10T and 6T XOR-XNORs and TG, 2T multiplexers, respectively. Figure 2 depicts the suggested 4-2 compressor gate-level architecture.

4. RESULTS

This section compares efficiency against both precise and approximate 4-2 compressors. Spectre from Cadence Design Systems is used for all of the simulations. 45nm and 90nm CMOS technology nodes are used to mimic every circuit. The performance of the proposed method is evaluated using MRED, NMED, power, transistor count, and delay compared with existing techniques.

4.1. Performance analysis

The NMED is the MED standardized to the particular design's highest efficiency. In many approximation applications, the difference between exact and approximate results exceeds their relative differences. The mean relative error distance (MRED) for every N-bit approximation adder is given in (7),

$$MRED = \frac{1}{2^{2N}} \sum_{i=1}^{2^{2N}} \frac{ED_i}{M_i} \quad (7)$$

where M_i is the precise multiplication value an MED that represents the average error distance.

Normalized MED is given in (8),

$$NMED = \frac{1}{2^{2N}(2^N - 1)^2} \sum_{i=1}^{2^{2N}} ED_i \quad (8)$$

where ED is the error rate of the metric. CMOS logic operates in a static state, which means that the input voltage remains practically constant, where V_{cc} is the voltage delivered to a logic I_c, I_{cc} while is the static supply current.

4.2. Comparative analysis

In the proposed 4:2 compressor designs, the cost function (CF) is employed as a unified metric to assess overall design efficiency by integrating multiple performance parameters such as area, delay, power, and MRED. The CF, defined by (9), helps in quantitatively comparing the trade-offs between accuracy and hardware efficiency across various compressor architectures. This approach enables a holistic evaluation that extends beyond isolated metrics, ensuring that the proposed design achieves an optimal balance between computational accuracy and resource utilization.

$$CF = Area\ x\ Delay\ x\ Power\ x\ MRED \quad (9)$$

Table 2 presents the average power consumption results of both regular and proposed 4:2 compressor architectures implemented under 90 nm and 45 nm CMOS technology nodes. It can be observed that the proposed designs consistently exhibit lower power consumption compared to their regular counterparts in both technology scales. This significant reduction is attributed to transistor-level optimization, where simplified logic paths and reduced switching activities contribute to minimizing dynamic power losses.

Table 2. Average power of 4:2 compressors

Name	Compressor	Power (µm^2)			
		Regular		Proposed	
		90nm	45nm	90nm	45nm
Design 1	10T XNOR-XOR+TG MUX	66.7	296.1	27.9	135.2
Design 2	6T XOR-XNOR+TG MUX	63.2	278.3	25.1	121.7
Model 3	10T XNOR-XOR+2T MUX	60.1	195.1	22.4	78.7
Model 4	6T XOR-XNOR+2T MUX	58.4	128.5	0.78	64.2

Figure 4 shows the exact and proposed transistor counts for the 4-2 compressor designs. The four designs specified in Figure 4 have been constructed using 10 and 6-transistor XOR-XNOR circuits, and two input multiplexers are based on a transmission gate and 2 transistors. On comparison, the transistor count has been transformed to half between regular and proposed designs, that is, 50% advancement in design intricacy. Figure 4 shows the number of transistors in a quasi-finite 4:2 compressor over three designs in 90nm and 45nm technology nodes.

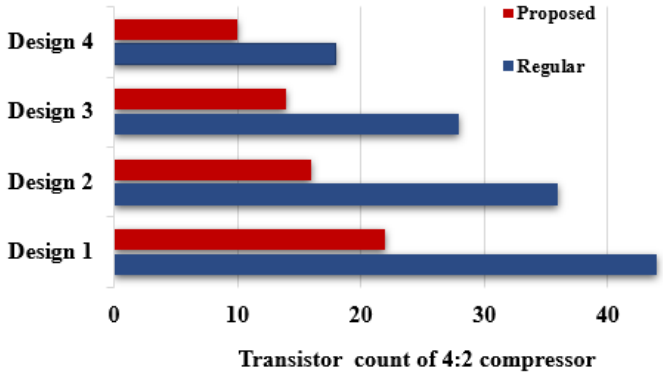

Figure 4. Transistor count of 4:2 compressor

Figure 5 illustrates the power delay product (PDP) of regular and proposed 4:2 compressor designs under both 90 nm and 45 nm CMOS technology nodes. It can be clearly observed that all proposed designs exhibit significantly lower PDP compared to their regular counterparts, confirming enhanced energy efficiency. The observed PDP improvement at the 45 nm node indicates that technology scaling, coupled with approximate design optimization, effectively enhances energy efficiency while maintaining reliable computational performance. Hence, the proposed compressors demonstrate a remarkable reduction in total energy consumption per operation, validating their suitability for low-power arithmetic and signal processing circuits.

In Figure 6, compared to existing designs, the proposed ones are quicker when the two technology nodes have been compared independently, and the speed increases as it descends from design 1 to design 4 in

90 nm and 45 nm nodes. Among all the architectures, design 3 and design 4 show the minimum delay values due to simplified transistor structures and reduced logic depth in the critical path. The overall delay trend demonstrates that the proposed compressors not only improve speed performance but also sustain stability under technology scaling.

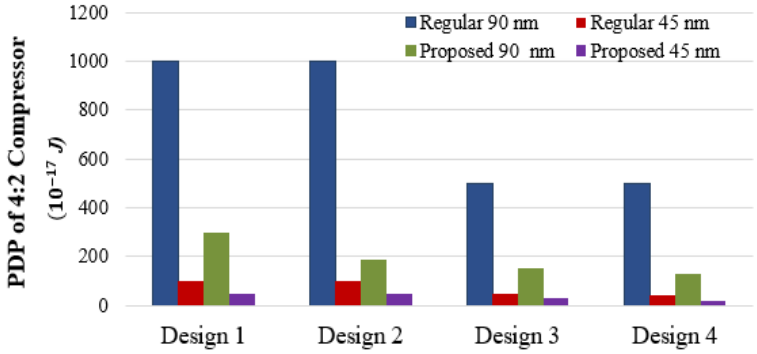

Figure 5. Power delay product of 4:2 compressor

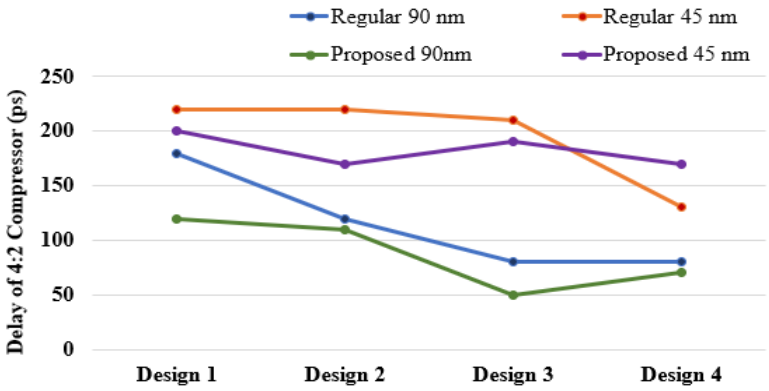

Figure 6. Delay of 4:2 compressors

4.3. Discussion

The proposed model is most suited for error-resistant applications. Converter transistors are effectively scaled to reduce power consumption, while the transmission gate transistors are tailored to improve compressor speed. End users should select designs based on the accuracy, power, and acceptable error ranges during simulation. At 45nm, the proposed design reduces power by 51.4% while reducing latency by 26.45%. Overheads are minimal in terms of accuracy degradation, measured through MRED and NMED.

5. CONCLUSIONS

In this paper, we realized the exact and proposed 4-2 compressor architecture, including 10T and 6T XOR-XNOR gates, transmission gate-based MUX, and two-transistor multiplexer blocks. For this reason, precision is not substantial in applications; approximations are enforced in regular compressors by considering Boolean expressions and truth tables, such that the proposed approximated compressor is more prominent than the regular ones in the perspectives of power and speed. A comparison was made between the actual approximation 4-2 compressor, showing 51.4% power reduction and 26.45% delay reduction for 45nm technology.

ACKNOWLEDGMENTS

The author would like to express his heartfelt gratitude to the supervisor for his guidance and unwavering support during this research for his guidance and support.

FUNDING INFORMATION

No financial support.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Jabez Daniel Vincent David Michael	✓			✓	✓	✓		✓	✓	✓		✓	✓	
Anusha Gorantla	✓	✓	✓	✓	✓		✓		✓	✓	✓		✓	
Ahilan Appathurai		✓		✓		✓		✓	✓	✓	✓	✓		
Dinesh Ramachandran		✓	✓			✓	✓		✓	✓	✓	✓	✓	

C: **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

INFORMED CONSENT

I certify that I have explained the nature and purpose of this study to the above-named individual, and I have discussed the potential benefits of this study participation. The questions the individual had about this study have been answered, and we will always be available to address future questions.

ETHICAL APPROVAL

My research guide reviewed and ethically approved this manuscript for publishing in this journal.

DATA AVAILABILITY

Data sharing is not applicable to this article as no datasets we regenerated or analyzed during the current study.

REFERENCES

[1] M. Maleknejad, F. Sharifi, and H. Sharifi, "A fast and energy-efficient hybrid 4–2 compressor for multiplication in nanotechnology," *Journal of Supercomputing*, vol. 80, no. 8, pp. 11066–11088, 2024, doi: 10.1007/s11227-023-05857-1.

[2] D. Champla, G. A. Safdar, B. Muthukumar, and M. M. Sithik, "C-AVPSO: Dynamic load balancing using African vulture particle swarm optimization," *International Journal of Data Science and Artificial Intelligence*, vol. 1, no. 2, pp. 1–9, 2023.

[3] M. J. Prajwala, K. Desai, and L. He, "Verification of NAND flash controller," in *Lecture Notes in Engineering and Computer Science*, 2022, vol. 2244, pp. 70–76.

[4] B. Sivasankari, M. Shunmugathammal, A. Appathurai, and M. Kavitha, "High-throughput and power-efficient convolutional neural network using one-pass processing elements," *Journal of Circuits, Systems and Computers*, vol. 31, no. 13, Sep. 2022, doi: 10.1142/S0218126622502267.

[5] M. I. Kollannur and S. Oudaya Coumar, "TFIE: three-four inexact adder based 4:2 and 5:2 compressor for high performance approximate booth multiplier," *International Journal of Electronics*, pp. 1–24, 2025, doi: 10.1080/00207217.2025.2500084.

[6] R. Thatikonda, "Walmart's electronic data interchange based supply chain performance enhancement using long short-term memory," *International Journal of Computer and Engineering Optimization*, vol. 2, no. 2, pp. 44–50, 2024.

[7] R. Nishanth, C. H. Sulochana, A. S. Radhamani, and A. Ahilan, "Design of imprecise compressor applications based on Hazy-Multipliers," *Journal of Intelligent and Fuzzy Systems*, vol. 44, no. 5, pp. 8725–8741, 2023, doi: 10.3233/JIFS-220418.

[8] P. Balasubramanian, R. Nayar, and D. Maskell, "An approximate adder with reduced error and optimized design metrics," in *2021 IEEE Asia Pacific Conference on Circuits and Systems, APCCAS 2021 and 2021 IEEE Conference on Postgraduate Research in Microelectronics and Electronics, PRIMEASIA 2021*, 2021, pp. 21–24. doi: 10.1109/APCCAS51387.2021.9687757.

[9] A. M. Dalloo, A. Jaleel Humaidi, A. K. Al Mhdawi, and H. Al-Raweshidy, "Approximate computing: Concepts, architectures, challenges, applications, and future directions," *IEEE Access*, vol. 12, pp. 146022–146088, 2024, doi: 10.1109/ACCESS.2024.3467375.

[10] Y. J. Pavitra and J. Manikandan, "Design of compressor-based multipliers using simulated annealing for arithmetic logic unit," *Neural Computing and Applications*, pp. 1–11, 2025, doi: 10.1007/s00521-025-10981-5.

[11] L. Maddisetti, R. K. Senapati, and J. V. R. Ravindra, "Image multiplication with a power-efficient approximate multiplier using a 4:2 compressor," in *Advances in Image and Data Processing using VLSI Design, Volume 1*, Bristol, UK: IOP Publishing, 2021, pp. 11–13. doi: 10.1088/978-0-7503-3919-3ch13.
[12] J. Gu and Y. Kim, "Design and analysis of approximate 4-2 compressor for efficient multiplication," *IEIE Transactions on Smart Processing and Computing*, vol. 11, no. 3, pp. 162–168, 2022, doi: 10.5573/IEIESPC.2022.11.3.162.
[13] T. S. A. Teja, G. Sai Teja, J. Ravindra, and L. Maddisetti, "High speed multiplier using embedded approximate 4-2 compressor for image multiplication," in *2022 1st International Conference on Artificial Intelligence Trends and Pattern Recognition, ICAITPR 2022*, 2022, pp. 1–5. doi: 10.1109/ICAITPR51569.2022.9844191.
[14] S. Karunamurthi, B. R. Jammu, N. Bodasingi, S. Veeramachaneni, and N. Mahammad S, "Image multiplication using novel 4:1 approximate compressor," *IETE Journal of Research*, vol. 70, no. 11, pp. 8242–8254, 2024, doi: 10.1080/03772063.2024.2369258.
[15] "Design of novel high speed energy efficient robust 4:2 compressor," *Journal of VLSI circuits and systems*, vol. 6, no. 2, Jan. 2024, doi: 10.31838/jvcs/06.02.05.
[16] A. Singh, A. V. Reddy, M. U. Kumar, E. Chitra, V. Marudhai, and R. Mishra, "Design of a 4-2 compressor-based approach for efficient approximate multiplier design," in *2024 IEEE International Conference on Information Technology, Electronics and Intelligent Communication Systems, ICITEICS 2024*, 2024, pp. 1–7. doi: 10.1109/ICITEICS61368.2024.10625587.
[17] S. Shetkar and S. Koli, "Area, power efficient Vedic multiplier architecture using novel 4:2 compressor," *Sadhana - Academy Proceedings in Engineering Sciences*, vol. 48, no. 4, p. 216, 2023, doi: 10.1007/s12046-023-02274-1.
[18] H. Raghuram, Vishnu, B. Vaishak, and B. S. Premananda, "Design and analysis of power and area efficient 4-2 compressor circuit for tree multiplier," in *7th IEEE International Conference on Computational Systems and Information Technology for Sustainable Solutions, CSITSS 2023 - Proceedings*, 2023, pp. 1–6. doi: 10.1109/CSITSS60515.2023.10334133.
[19] S. Skandha Deepsita and S. K. Noor Mahammad, "Low power, high speed approximate multiplier for error resilient applications," *Integration*, vol. 84, pp. 37–46, 2022, doi: 10.1016/j.vlsi.2022.01.001.
[20] S. Jeon, J. Jeon, Y. Lee, and Y. Kim, "New approximate 4:2 compressor for high accuracy and small area using MUX logic," in *2024 International Conference on Electronics, Information, and Communication, ICEIC 2024*, 2024, pp. 1–3. doi: 10.1109/ICEIC61013.2024.10457270.
[21] S. Y. Sridevi and K. Ragini, "Design of high performance approximate redundant binary multiplier using 4:2 & 5:2 compressors," in *AIP Conference Proceedings*, 2021, vol. 2407, no. 1. doi: 10.1063/5.0074136.
[22] Z. A. Zuhair and E. A. Al-Sabawi, "Design and evaluation of high-speed approximate multipliers based on improved error distance 4:2 compressors for error resilient image applications," *International Journal of Intelligent Engineering and Systems*, vol. 18, no. 1, pp. 422–445, 2025, doi: 10.22266/ijies2025.0229.31.
[23] L. Sayadi, S. Timarchi, and A. Sheikh-Akbari, "Two efficient approximate unsigned multipliers by developing new configuration for approximate 4:2 compressors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 4, pp. 1649–1659, 2023, doi: 10.1109/TCSI.2023.3242558.
[24] D. Rostami, M. Eshghi, and Y. S. Mehrabani, "Low-power and high-speed approximate 4:2 compressors for image multiplication applications in CNFETs," *International Journal of Electronics*, vol. 108, no. 8, pp. 1288–1308, 2021, doi: 10.1080/00207217.2020.1858973.
[25] R. Bhandari, "Design and analysis of approximate 4:2 compressors for high performance multiplier." 2024. doi: 10.22541/au.172845773.36403549/v1.
[26] U. Anil Kumar, S. K. Chatterjee, and S. E. Ahmed, "Low-power compressor-based approximate multipliers with error correcting module," *IEEE Embedded Systems Letters*, vol. 14, no. 2, pp. 59–62, 2022, doi: 10.1109/LES.2021.3113005.
[27] S. Mariserla, T. V Murthy, and K. Pradeep, "High speed VLSI architecture of approximate multiplier using majority logic." *International Journal of Research and Analytical Reviews*, 2024.

BIOGRAPHIES OF AUTHORS

Jabez Daniel Vincent David Michael is working as an assistant professor in the Department of Electronics and Communication Engineering, Dr. Sivanthi Aditanar College of Engineering, Tiruchendur. He received his B.E. degree in electronics and communication engineering from Anna University, Chennai, and M.E. degree in embedded systems technologies from Anna University, Chennai. He completed his doctorate in the area of VLSI signal processing at Anna University Chennai. He has published a few national and international journal and conference papers and participated in several international conferences. His research interests include signal processing, embedded systems, and neural networks. He can be contacted at jabezdaniel@gmail.com.

Anusha Gorantla received her bachelor's degree in electronics and communication engineering in 2006 from JNTU Hyderabad, Andhra Pradesh, India. She received an M.Tech. in VLSI design in 2008 and a Ph.D. degree in information and communication engineering in 2018 from Anna University, Chennai, Tamil Nadu, India. She is currently working as an associate professor in the Department of Electronics and Communication Engineering, Raghu Engineering College, Visakhapatnam, Andhra Pradesh, India. Her research areas include low-power VLSI design, approximate computing, and image processing. She has served as a reviewer for various reputed international journals. She can be contacted at anushagorantla3@gmail.com.

Ahilan Appathurai received his Ph.D. from Anna University, India, and is working as an associate professor in the Department of Electronics and Communication Engineering at PSN College of Engineering and Technology, India. His areas of interest include FPGA prototyping, computer vision, the Internet of Things, cloud computing in medical, biometrics, and automation applications. He has served as a guest editor for several journals of Elsevier, Bentham, and IGI publishers, and has contributed original research articles in IEEE Transactions, SCI, SCIE, and Scopus-indexed peer-reviewed journals. He has presented papers at various international conferences such as ASQED (Malaysia) and ESREF (France). He serves as a reviewer for IEEE Industrial Informatics, IEEE Access, Measurement, Multimedia Tools & Applications, Computer Networks, Medical Systems, Computer & Electrical Engineering, Neural Computing and Applications, Cluster Computing, and IET Image Processing. He holds IEEE and ISTE memberships and has worked as a research consultant at TCS, Bangalore, where he guided many computer vision and Bluetooth Low Energy projects. He also has hands-on programming experience in MATLAB, Verilog, and Python at various technical institutions around India. He can be contacted at listentoahil@gmail.com.

Dinesh Ramachandran has been in teaching for 18 years and is currently working as a professor in the Department of Electronics and Communication Engineering at Excel Engineering College, Komarapalayam, Namakkal, India. He received his B.E. degree in electronics and communication from Bharathidasan University, India; M.E. degree in optical communication from Anna University, India; M.B.A. degree from Madurai Kamaraj University, India; and Ph.D. in VLSI from Sathyabama University. He has published 25 technical papers in international conferences and journals in the areas of optical communication, VLSI, IoT, and signal processing. He has published six design patents in India and authored books on VLSI, optical communication, wireless networks, and ChatGPT. He has also acted as a reviewer for several IEEE international conferences. He is a lifetime member of ISTE. His research interests include low-power VLSI, clock synchronization, and ADPLL. He can be contacted at dinesh.is@hkbk.edu.in.