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Designing high power efficient finite impulse response filters with three-four inexact adder-integrated Booth multiplier

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ABSTRACT

Finite impulse response (FIR) filters are widely utilized in several applications in digital signal processing, including data transmission, photography, digital audio, and biomedicine. It is necessary to use high sample rates for FIR filters, while moderate sample rates are needed for low-power circuits. To solve these problems, a Booth multiplier based on three-four inexact adder-based multiplication (TFIE-BM) was proposed. The goal of the proposed TFIE-based FIR Booth multiplier is to lower area usage, latency, and power consumption. The proposed method utilizes the spotted hyena optimizer (SHO) to find the optimal filter coefficient (FC) by minimizing the pass power consumption and Transition bandwidth. Moreover, a high-performance three-four inexact adder (TIFE adder) has been introduced, which uses fewer XOR gates for sum and carry generation, indicating that the logic has been simplified to reduce hardware complexity. By increasing speed and decreasing the FIR filter's critical path delay, a modified Booth multiplier that uses a 5:2 compressor is introduced. The overall delay of the proposed approach is 23.4%, 18.7%, 12.3%, and 5.7% lower than that of the Radix-4 Booth multiplier, CSA Booth multiplier, hybrid multiplier, and traditional Booth multiplier, respectively.

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1. INTRODUCTION

In the current generation, technology requires reducing the size of electronics equipment as well as enhancing of speed of devices [1]. Applications that make use of digital filters the most include those for image, video, and speech processing. Digital filters with finite impulse response (FIR) and infinite impulse response (IIR) are also available. Due to its superior stability and simple design, the FIR filter is suggested for the previously listed applications [2]. The linear phase property and robustness of FIR filters make them widely used in digital signal applications. Designing DSP systems requires a high-performance system; the most important factors are low power consumption and reduced clip size. FIR filters are crucial for image processing, mobile communications, and audio processing applications due to their inherent reliability and linear phase properties [3], [4]. In the present day, a number of FIR filter designs have been released, some for low-speed, some for high-speed, as well as others for low power consumption [5], [6].

Adder and multiplier circuits typically have the greatest impact on the delay and power performance of FIR filter designs. Multipliers typically dictate how long the FIR filter design takes to execute [7]. For the purpose of designing a delay with effective FIR filters, high-speed multipliers are therefore needed. The

multiplier is the slowest block in the adder and has a significant impact on the performance of the FIR filter [8]. The latency will be decreased by the Finite Impulse Response Filter's employment of the Booth Multiplier and carry choose adder [9], [10]. By using this method, the total area and delay are decreased by half due to the reduction of accumulations [11]. Incorporating the multiplication, addition, and signal delay building components is necessary for the FIR filter [12]. The creation of partial products (PP), their reduction, and their ultimate addition are typically needed when multiplying two binary values [13]. A multiplier requires additional hardware and a longer processing time for these operations [14], [15].

Recently, a variety of delay-efficient adders have been created to meet the requirements of real-time applications [16]. Because of this, the traditional FIR-based design performs poorly in terms of latency and speed [17]. But efficiency and area overhead typically present competing limits; thus, increasing speed largely benefits larger areas [18]. Over the past ten years, many Booth multiplier and Booth-based FIR designs have been introduced. Radhakrishnan *et al*. [19] proposed a filtering application that incorporated a multiple-and-accumulate (MAC) device with a modified Booth multiplier and hybrid adder in order to boost speed and lower power consumption. Utilizing Cadence Virtuoso's 45 nm, 180 nm, and 90 nm TSMC computing library, efficiency metrics such as delay and energy use are assessed. More effective Booth multiplier based on a FIR architecture that is reliable and uses little energy in [20]. The slices, number of gates, and LUTs of the suggested research are better than those of other earlier designs. An enhanced Booth for a 16-Tap FIR filter and a Radix-4 Booth multiplier were employed in [21]. In 2022 the Wallace Tree multiplier [22], according to the 7–3 and 8–3 compressors, was created to further reduce delay. Using 7–3 and 8–3 compressors, the suggested 8-bit FIR filter design with Wallace tree multipliers achieves a delay of 4.202 ns and 3.861 ns, accordingly, which is 29% and 34% lower than the standard FIR filter.

An optimized FIR Filter is introduced in [23] that uses a Booth multiplier and CSA to cut down on latency. The proposed method utilizes a Verilog HDL-designed, Xilinx 14.7 Vivado-implemented 15-tap lowpass filter. The Booth multiplier's lower operating frequency, lower power consumption, and lower latency make it an excellent choice for low-voltage and low-power VLSI scenarios. Additionally, a Booth multiplier, multibit flip-flops, and data-driven clock gating are introduced in [24] to optimize clock delay, control clock skew, and improve routing source utilization. Using hybrid adders and multipliers, [25] presented a hybrid FIR filter in 2023 to speed up the signal processing system. The suggested FIR filter was created using the Xilinx ISE simulator, tested functionally, and then integrated into Spartan 6 FPGA boards. The results indicate that the suggested adder with array multiplier lowers the FIR filter's latency by 26.51%, 15.59%, and 15.83%, when compared to conventional CSA, CLA, and CSA-BK-BEC.

From recent research, the existing techniques face challenges like power consumption, especially in low-voltage applications that were minimizing energy, enhancing scalability without compromising speed or area efficiency. Higher power consumption is associated with FIR filters that use traditional multipliers and adders, especially in large-scale or high-performance FIR filters. To overcome these issues, a three-four inexact adder-based Booth multiplier in an FIR filter has been proposed.

The proposed method utilizes the spotted hyena optimizer (SHO) to determine the best filter coefficient (FC) by reducing pass power usage and transition bandwidth. Spotted hyena optimizer (SHO) will be used to discover the best FCs by lowering the transition bandwidth and power consumption. The high-performance three-four inexact adder (TIFE adder) has been proposed, which uses fewer XOR gates for sum and carry generation, indicating that the logic has been simplified to reduce hardware complexity. A modified Booth multiplier is introduced that makes use of a 5:2 compressor to reduce the number of partial products bits more efficiently by enhancing speed and reducing the critical path delay of the FIR filter. Additionally, power consumption is much decreased by the improved Booth multiplier that uses an adder in the FIR design. The key finding of the proposed strategy is that, in comparison to traditional and existing multiplier designs, it greatly enhances the performance of FIR filters by lowering power consumption by 69.5%, area usage by up to 58.45%, and delay by 73.8%.

The research questions for the proposed method are: i) How can FIR filter design be optimized for higher speed, lower delay, and power efficiency? ii) Can a three-four inexact adder-based Booth multiplier (TFIE-BM) with SHO significantly improve area, delay, and power consumption in FIR filters? iii) How does the proposed multiplier architecture improve critical path delay and reduce partial product generation?

The remaining tasks are arranged; section 2 explores the existing method utilized for FIR design. The specifics of the suggested filter structure are covered in section 3. In section 4, the design's result is evaluated and explored. Section 5 finally concludes the paper.

2. PROPOSED NOVEL FIR METHOD

In this section, a novel TFIE-BM in the FIR filter has been proposed to enhance speed and reduce the critical path delay. Signal processing fields like image, audio, and video processing, as well as medical processing, use the FIR filter, which is developed from the impulse response with a finite time period. We

aim to use a carry skip adder in our suggested work, and the main focus is on designing a high-speed, low-power filter. The capacity of a FIR filter to remove unnecessary noise from signals, which can be generated in discrete or continuous time, is its primary advantage. The standard formula for a FIR filter is as (1).

$$Y_n = \sum_{a=1}^{n-1} fc(i)X(n-1) \quad (1)$$

In this case, X stands for the input data passed through the filter, Y_n indicates the filter output, fc is the filter coefficient, and m number of FC. T Figure 1 shows the FIR filter's construction with the recommended multiplier, delay, and adders. The frequency response of the FIR filter must have as minimal ripple as feasible in the pass and stop bands. In order to minimize ripples, the work focuses on designing FIR filters based on the difference between the anticipated and actual frequency response. By using fewer FIR FCs, the FIR filter's power consumption should be reduced. To find the best FCs, researchers created the SHO. Providing ideal FCs by reducing power consumption and ripples in the pass and stop bands is the main objective of this technique. Due to their partial product (PP)-dependent delay, FIR filters require more power because they are programmed in an FPGA with optimal coefficients.

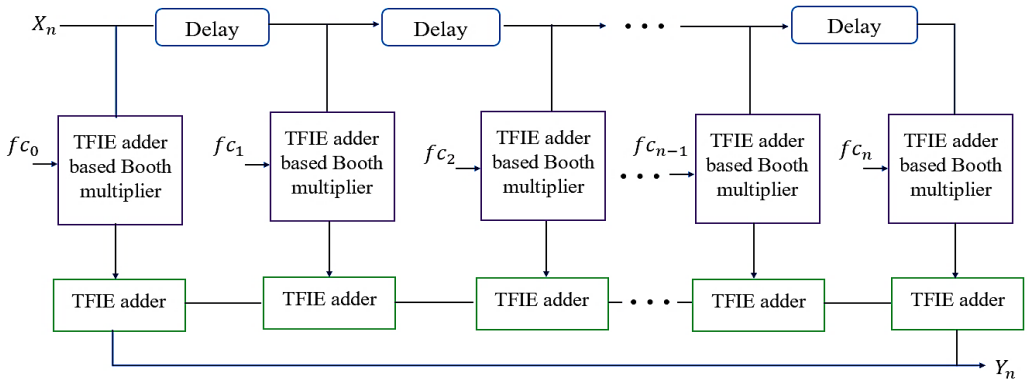

Figure 1. Proposed novel FIR design

2.1. SHO based FIR filters design

The FIR filter had to address the issue of band ripple and halt pass band while keeping power consumption low. Therefore, choosing the best FC is necessary to create a distortion-free FIR filter design. In our proposed study, the ideal FC to improve the functional objective has been identified by building the filter with SHO in terms of absolute response to the frequency of the FIR filter.

An optimization method inspired by spotted hyenas' hunting habits is called the SHO. Multimodal optimization and convergence speed are two difficult optimization issues that SHO can handle. To get the optimal filter coefficient, one can express objective functions like power consumption and transition width (TrW) in terms of a FIR filter that has been constructed and desired. The FIR filter design reduces power by defining the objective function in relation to Hamming distance.

$$F_1 = \sum_{b=1}^{P} \pi(Coeff_b, coeff_{b+1}) \quad (2)$$

In this case, $\pi(Coeff_b, coeff_{b+1})$ uses binary numbers to display the HD between each FC, with P standing for the filter order. The pass and ripple band can be used to declare the objective function of TW, which is assessed as (3):

$$F_1 = \sum_{p=1}^{P_i} abs\left[abs\left(\left|G_i\left(\frac{\pi p}{Q}\right)\right| - 1\right) - \mu_i\right] + \frac{C\pi}{Q}(Q_d - Q_i) + \sum_{q=1}^{Q_d} abs\left[abs\left(\left|G_q\left(\frac{\pi p}{Q}\right)\right| - 1\right) - \mu_d\right] \quad (3)$$

where TrW is given a weight based on an unchanged value, C. Using the optimization process, the FC is found using (2) and (3). The population's finest FC is first identified, and other people adjust their perspectives in accordance with it. Equation (4) models the surrounding mechanism.

$$\overrightarrow{S_{eq}} = \left|\vec{W} \cdot \overrightarrow{R_{dq}}(q) - \vec{R}(q)\right| \quad (4)$$

$$\vec{R}(q+1) = \overrightarrow{R_{dy}}(q) - \vec{C} \cdot \overrightarrow{S_{eq}} \quad (5)$$

$\vec{R}(q+1)$ denotes the FC current location in the current coefficient. The algorithm iteration is q, and hyenas use this equation to gauge the distance to their prey, surrounded by specific mechanisms. Equations (6) and (7) calculate vector coefficients $\overrightarrow{W}$ and $\vec{C}$, using position vectors and element-wise multiplication.

$$\overrightarrow{W} = 2 \cdot \overrightarrow{\iota g_1} \quad (6)$$

$$\vec{C} = 2\vec{f} \cdot \overrightarrow{\iota g_2} - \vec{f} \quad (7)$$

Equation (5) shows that $\overrightarrow{\iota g_1}$ and $\overrightarrow{\iota g_2}$ are random vectors in the interval (0, 1), and that h drops linearly from 5 to 0 during the iteration time. An increased number of iterations is necessary to increase efficiency. In order to identify the top search agent, other search agents' band together and update the best FC they have found which are given in (8).

$$\overrightarrow{U_{eq}} = \vec{R}_k + \vec{R}_{k+1} + \cdots + \vec{R}_{k+N} \quad (8)$$

whereas the other filter coefficient location is indicated by $\vec{R}_k$. Equation (10) is used to calculate the number of hyenas, which is displayed in Parameter M.

$$M = count_{ns}\left(\vec{R}_{eq} + \vec{R}_{eq+1} + \vec{R}_{eq+2}, \ldots\ldots, \left(\vec{R}_{eq} + \vec{N}\right)\right) \quad (9)$$

The ns parameter in (25) specifies the total number of solutions as well as all feasible solutions., where $\vec{N}$ is a random vector in the interval (0.5,1). The parameter $\overrightarrow{C_{hy}}$ represents a set of the ideal solution's number M. The worth of the path is decreased with the purpose of creating a mathematical model for the target attack. The vector can have its value reduced from 5 to 0 during an iteration by reducing the change in the vector C. The pack of untainted hyenas is forced to outbreak the target if the value of C is |C| < 1,

$$\vec{R}(q+1) = \frac{\overrightarrow{U_{eq}}}{M} \quad (10)$$

The best agent's position determines how the other search agents are positioned. During each iteration, the algorithm evaluates the fitness of each filter coefficient. The best solution found so far is updated by comparing the fitness values. Until the worldwide optimal FCs are selected, the same process will be performed n times after evaluating the best FC currently in use. After determining the optimal FC, a modified parallel-architecture Booth multiplier utilizing TFIE adder-based technology is shown in order to reduce power consumption and latency.

2.2. TFIE adder-based Booth multiplier

Since FIR filters are only sometimes utilized in applications, they must be multiplied and produce more partial products. In FIR filter designs, an excess of products results in a longer interval between stages. In earlier studies, a greater number of adders was employed to lower power and latency.

2.2.1. TFIE adder

The simplest way to implement binary addition, in which the carry-in to a bit is given by the carry-out of the preceding bit, is through the proposed three-four inexact adder (TFIE adder). Each bit generates carryout and total, which are then passed as carry-in to the following bit. Figure 2 depicts the circuit diagram of the TFIE adder, which consists of three inputs: A, B, and C (where C is the carry-in). Equations (11) and (12) are used to compute the sum and carry.

$$\text{Sum} = (\text{A}'(\text{B} + C_{in}) + \text{B}C_{in}) \quad (11)$$

$$Carry = \text{AB} + \text{B}C_{in} + \text{A}C_{in} \quad (12)$$

The proposed TFIE adder uses a minimal number of logic gates (XOR, AND, OR) to compute both the sum and carry, which simplifies the overall design. The circuit may execute addition with less gate delays than a standard adder design by combining XOR gates for the sum and a mix of AND/OR gates for the carry.

This lowers the overall propagation delay. The overall reliability of the system is increased by having fewer gates and a simpler design, which reduces the possibility of failure sites.

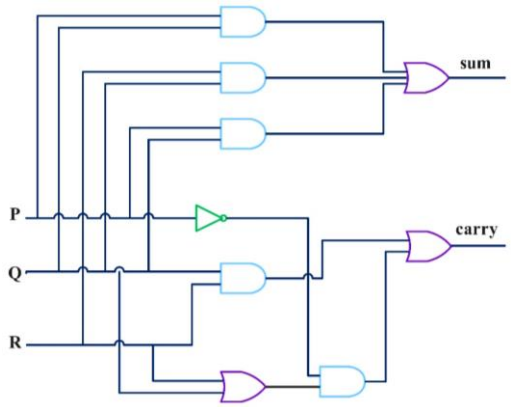

Figure 2. Circuit diagram of TFIE adder

2.2.2. Enhanced Booth multiplier

In the proposed method, a compressor-based multiplier focuses on reducing PP generated during multiplication by using compressors (like the 5:2 compressor in this case) to sum multiple bits simultaneously. The design shown in the diagram aims to speed up the partial product summation process using compressors, half adders, and full adders, without changing the encoding of the input numbers, as done in Booth's algorithm. The modified Booth multiplier is depicted in Figure 3. Here, the 5:2 compressor reduces five input bits and two carry-in bits into two output bits (a sum and a carry), significantly speeding up the summation of the partial products. Compressors are used to handle the large PP in multipliers, reducing them efficiently.

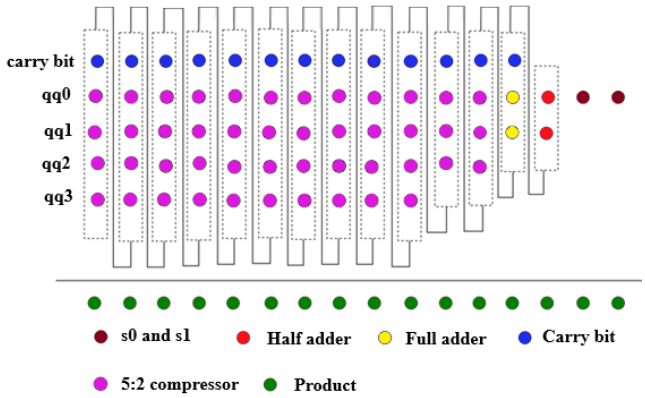

Figure 3. Modified Booth multiplier

Figure 3 shows different colors to represent various components involved in the multiplier's architecture. Purple circles represent the 5:2 compressors, which reduce five input bits and two carry bits into two output bits (sum and carry). Red circles indicate half adders, which add two input bits and generate a sum and a carry. Yellow circles represent full adders, used when three bits are added (two inputs and a carry). Blue circles show the carry bits, which propagate through different columns in the array to the next higher bit position. Brown circles denote the final outputs, S0 and S1, from the summation stages, and green circles represent the final product bits generated as a result of the multiplication. This color coding helps differentiate the components and their roles in reducing and summing partial products during the multiplication process.

3. RESULT AND DISCUSSION

The proposed innovative FIR filter design has been carried out in Verilog coding by employing the Xilinx ISE 14.5 tool. By contrasting its efficacy with that of alternative metaheuristic techniques, the suggested FIR filter's value in selecting the best FC is illustrated. Additionally, a number of multiplier and adder designs are taken into consideration while analyzing the hardware complexity of the proposed FIR filter.

Figure 4 shows the convergence behavior of both the proposed and existing methods. By taking into account fewer repetitions, the suggested SHO methodology produces optimal FCs with fewer ripples as compared to current methods. This is a result of the SHO technique's exploration and exploitation behavior. Because adaptive step size method is paired with position update equations, finding the best FCs in fewer iterations is made possible. In order for the suggested approach to converge quickly and with few iterations. After the best FC was selected using SHO, the FIR filter was created using a Booth multiplier based on TFIE-BM.

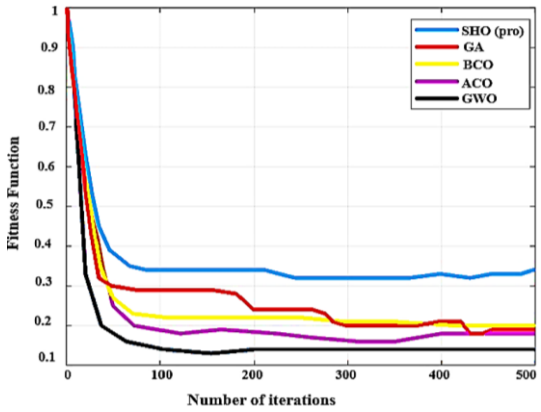

Figure 4. Convergence analysis

Table 1 shows the comparative analysis of the traditional Booth multiplier, Radix-4 Booth multiplier [21], CSA and Booth multiplier [22], and hybrid multiplier [25] with certain existing multipliers have confirmed the efficacy of the suggested TFIE-BM-based Booth multiplier. Because radix-2 encoders are used, the space and delay of the traditional Booth multiplier have increased. We designed this particular multiplier. Using 183 slices, 372 LUTs, 16.21 ns of delay, and 0.246 W of power consumption, the traditional Booth multiplier is the most resource-intensive. The proposed TFIE-BM achieves the best performance with only 39 slices, 63 LUTs, the shortest delay of 4.217 ns, and the lowest power consumption at 0.075 W, offering significant improvements over the other designs in both speed and efficiency.

Table 1. Comparison of the proposed multiplier at the 32x32 level

Multiplier	Number of slices	LUTs	Delay (ns)	Power (W)
Conventional Booth multiplier	183	372	16.21	0.246
Radix-4 Booth multiplier [21]	142	207	12.65	0.148
CSA and Booth multiplier [22]	107	185	8.475	0.105
Hybrid multiplier [25]	61	115	5.987	0.095
Proposed TFIE-BM	39	63	4.217	0.075

Figure 5 shows the area comparison of the proposed design with the prior multiplier for 8×8 level. In comparison to existing methods, the proposed TFIE-BM reduces area usage. Compared to the Radix-4 Booth multiplier, which consumes around 90,000 μm², the TFIE-BM reduces area by 72.22%. When compared to the CSA and Booth multiplier (70,000 μm²), the reduction is 64.29%. Against the hybrid multiplier (45,000 μm²), the TFIE-BM achieves a 44.44% reduction. These percentage reductions highlight that the proposed TFIE-BM design is highly efficient, using far less area than its predecessors across all existing designs.

Figure 6 shows the comparative analysis of the area for the 16×16 level with proposed and existing methods. From the comparison, the conventional Booth multiplier has the highest area compared to other existing and proposed techniques. Finally, the proposed TFIE-BM shows the most substantial improvement, reducing the area by about 55%, 35.2%, 25.48%, and 10.8% compared with conventional Booth multiplier, Radix-4 Booth multiplier [21], CSA and Booth multiplier [22], and hybrid multiplier [25] design. This analysis highlights that the proposed TFIE-BM offers the most efficient area usage compared to all other methods.

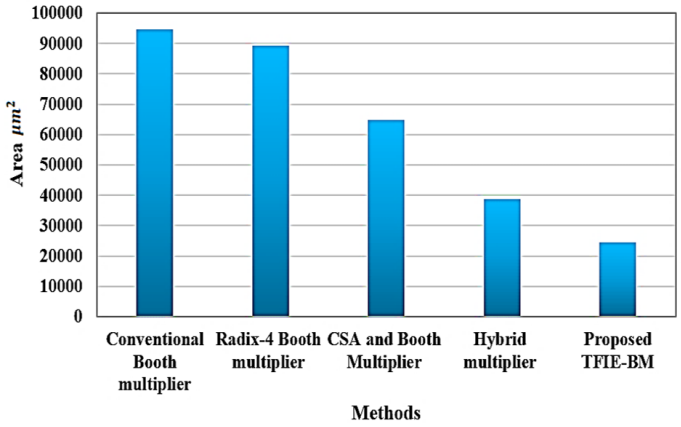

Figure 5. Comparison of area analysis for 8×8 level

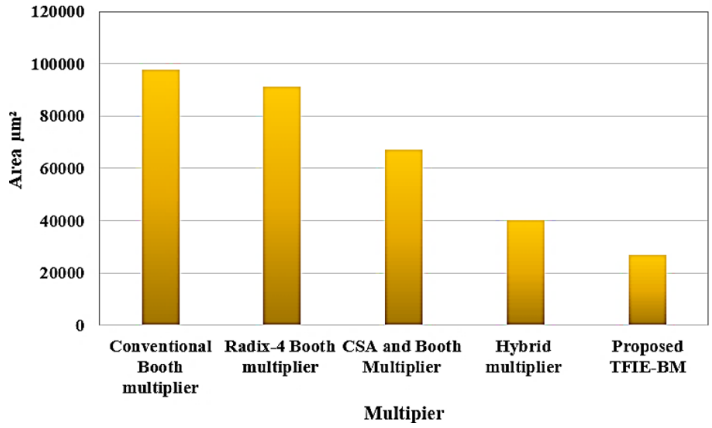

Figure 6. Comparison of area analysis for 16×16 level

Figure 7 shows the comparative analysis of the area for the 32×32 level with proposed and existing methods. From the comparison, the conventional Booth multiplier has the highest area compared to other existing and proposed techniques. Finally, the proposed TFIE-BM shows the most substantial improvement, reducing the area by about 58.45%, 38.15%, 29.48%, and 15.21% compared with the conventional Booth multiplier, Radix-4 Booth multiplier [21], CSA and Booth multiplier [22], and hybrid multiplier [25] design. This analysis highlights that the proposed TFIE-BM offers the most efficient area usage compared to all other methods.

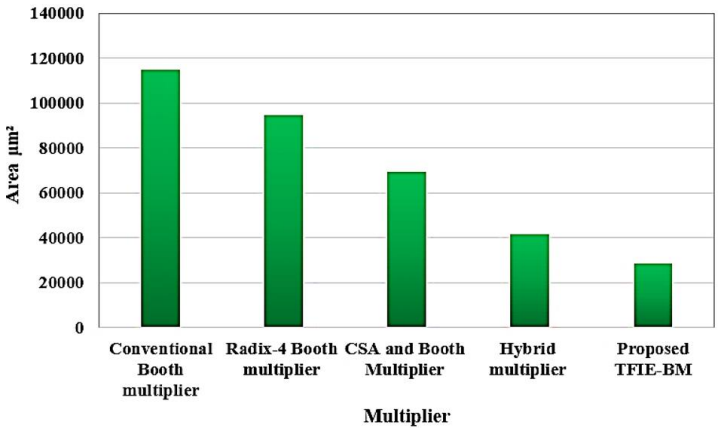

Figure 7. Comparison of area analysis for 32×32 level

3.1. Discussion

The Xilinx ISE 14.5 tool is being utilized for testing the suggested innovative FIR filter design using Verilog code. Performance metrics indicate a significant improvement when compared with proposed and existing methods. When choosing the best FCs, Figure 4 shows how the proposed SHO behaves in terms of convergence. Compared to other optimization techniques, the SHO shows faster convergence because of its effective exploration and exploitation capabilities. Significant speed and efficiency gains over the other designs are provided by the proposed TFIE-BM, which performs best with just 39 slices, 63 LUTs, the shortest latency of 4.217 ns, and the lowest power consumption of 0.075 W. Additionally, the delay caused by the advancement of high-speed addition and multiplication is decreased by the suggested FIR filter design. The proposed FIR filter is a feasible option for high-performance, low-power applications as, according to comparative studies, it reduces area by 58.45% and improves latency by 73.8% when compared to traditional Booth multipliers. Figures 5, 6, and 7 show the area analysis at various levels (8×8, 16×16, and 32×32), which shows the significant decrease in resource usage attained by the proposed TFIE-BM design. Overall, the numerical study demonstrates that the TFIE-BM architecture performs better in terms of scalability and efficiency. The outcomes confirm the proposed method's resilience and its capacity to resolve issues with conventional FIR filter designs in practical settings.

4. CONCLUSION

In this research, a novel TFIE-BM multiplier in FIR filter design has been proposed to reduce power consumption and delay, and save area. In order to minimize the pass power consumption and transition bandwidth, the suggested method makes use of the SHO to determine the ideal FC. Moreover, high performance TIFE adder has been introduced, which uses fewer XOR gates for sum and carry generation, indicating that the logic has been simplified to reduce hardware complexity. By increasing speed and decreasing the FIR filter's critical path delay, a modified Booth multiplier that uses a 5:2 compressor is introduced. This reduces the number of partial products bits more effectively. Additionally, the power consumption is much reduced by the improved Booth multiplier that uses an adder in the FIR architecture. To evaluate the effectiveness of the suggested approach, area, power, and latency simulations were performed using the Xilinx ISE 14.5 tool. Based on area, power, speed, and latency, the simulation findings depict that the suggested TFIE-FIR filter performs better than the designs. Overall, the recommended method has a shorter latency than the Radix-4 Booth multiplier, CSA and Booth multiplier, hybrid multiplier, and traditional Booth multiplier by 23.4%, 18.7%, 12.3%, and 5.7%, respectively. Future research will further reduce the energy consumption of the FIR filter by combining the Booth multiplier with advanced power reduction strategies like clock gating and dynamic voltage scaling (DVS).

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C : **C**onceptualization
M : **M**ethodology
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Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

INFORMED CONSENT

We certify that we have explained the nature and purpose of this study to the above-named individual, and we have discussed the potential benefits of this study participation. The questions the individual had about this study have been answered, and we will always be available to address future questions.

ETHICAL APPROVAL

The research guide reviewed and ethically approved this manuscript for publishing in this journal.

DATA AVAILABILITY

Data sharing is not applicable to this article as no datasets we regenerated or analyzed during the current study.

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